

Gate control of spin-orbit interaction in a nanowire gate-all-around FET with atomic-layer-deposited $\text{Al}_2\text{O}_3/\text{ZnO}$ gate-stack

Keiko Takase, Kouta Tateno, and Satoshi Sasaki
NTT Basic Research Laboratory, NTT Corporation,
3-1, Morinosato-wakamiya, Atsugi, Kanagawa 243-0198, Japan
Phone: +46-240-3181 E-mail: keiko.takase.wa@hco.ntt.co.jp

Abstract

Electrical control of spin-orbit interaction has attracted much attention in terms of novel application to quantum devices including spin FET and Majorana devices. Here, we demonstrate that the Rashba spin-orbit interaction is electrically tuned in a nanowire gate-all-around FET with all atomic-layer-deposited gate-stack, which can reduce interface states in the device and will be applied for future high-frequency technology. This opens up a way toward a prototype of high-frequency spin-orbitronics devices.

1. Introduction

The spin-orbit interaction (SOI) is one of the key elements that allows external electric fields to access electron spin. This has stimulated researchers to investigate application of the spin-orbit interaction for a future electronics such as a spin FET [1] and newly emerging fields of Majorana electronics [2]. Associated with this trend, gate control of the spin-orbit interaction in III-V semiconductor nanowire has been examined by many groups using various device structures, ranging from a conventional back- or top- gate [3,4] to a surrounding gate-all-around (GAA) structure using ionic electrolyte [5], the latter of which demonstrated high efficiency of SOI tuning owing to its unique structure.

Recently, we developed an InAs nanowire FET with a gate-all-around metal-oxide-semiconductor (MOS) structure [6]. This enables us to apply strong and homogeneous electric field, leading to large electrical tuning of the Rashba spin-orbit interaction with low gate voltage. While this device did not exceed the gate efficiency obtained for the ion-gate device, the MOS structure is useful for fast gate response that is necessary for practical application. However, this metallic GAA structure has room for improvement in terms of yields and future application to high frequency technology reaching to GHz and THz. Therefore it is required to develop new types of devices that can minimize screening effect and be suitable to operation at various frequency ranges.

Here, we report a gate control of the SOI for a gate-all-around InAs nanowire FET with *in-situ* atomic-layer deposition (ALD) growth of gate insulator and conductive ZnO around nanowire. *In-situ* growth of gate stack can reduce interface states in the device and thus can improve device performance. By conducting magnetotransport measurements, we find crossover from weak localization to weak antilocalization, indicating a significant electrical control of the SOI. The estimated gate efficiency of the SOI is as large as that for

our previous metallic GAA FET [6] and larger than those reported for two-dimensional III-V semiconductor Schottky FETs [7,8]. Considering the fact that ZnO is known to be transparent in the range of visible to far infrared (THz) regime [9], this type of device will contribute to further development in spin-orbitronics and, in the future, will serve as a hybrid device in which electron spin can be controlled through the SOI by electric field and by optical excitation.

2. Experimental Method

The gate-all-around FET was developed using InAs nanowire grown by MOVPE method using Au catalyst. We fabricate insulating Al_2O_3 (6 nm) and conductive ZnO (20 nm) layers successively around InAs nanowire with ALD technique, the structure of which is schematically shown in Fig. 1(a). The *in-situ* growth of insulating layer (gate insulator) and conductive layer (gate electrode) serves well to reduce contamination and possibly interface states in the device. Figure 1(b) shows transmission electron microscopy (TEM) image of InAs nanowire coated by Al_2O_3 and ZnO layers. Since we use ALD technique, we can find that these layers surround all the nanowire homogeneously even for the apex of nanowire. After the ALD growth, we etch the edges of coated nanowire, and deposit metal to make source and drain contacts. We emphasize that ZnO layer acts as gate electrode just as it is, since we grow n-doped conductive ZnO by ALD deposition. We here demonstrate the characterization of the DC properties and electrical control of the spin-orbit interaction for this type of nanowire FET, and perform measurements using standard DC techniques at temperature of around 1.5K.

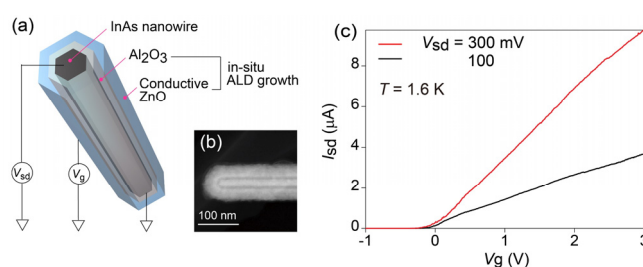


Fig. 1 (a) Schematic illustration of GAA InAs nanowire FET using Al_2O_3 and conductive ZnO layers grown by ALD method. (b) TEM image of the nanowire with ALD-grown layers. (c) Source-drain current vs gate voltage for different source-drain voltages.

3. Experimental Results

Figure 1(c) shows source-drain current (I_{sd}) as a function of gate voltage (V_g), which is measured at different source-drain voltage (V_{sd}) at temperature (T) of 1.5 K. With increasing V_g , we find that I_{sd} suddenly increases, corresponding to transistor DC transfer characteristics. The subthreshold swing is about 30 meV/dec, which is comparable to previously reported InAs nanowire FETs.

Having clarified FET characteristics, we measured magnetoconductance ΔG as a function of magnetic field (B). Here ΔG is defined as a difference from the zero-field conductance. The inset in Fig. 2 shows ΔG vs B . We note that the data shown in the inset are smoothed over with respect to magnetic field and gate voltage to exclude universal conductance fluctuation to obtain better fitting accuracy, as is usually done for previous papers. In addition, we average the data for negative and positive magnetic field for the same reason described above. As V_g is increased, we find that ΔG vs B shows a change from a dip to a peak structure, indicating that a transition from a weak localization to a weak antilocalization, the latter of which is reported to occur in the presence of the strong spin-orbit interaction.

To extract the spin-orbit length that is directly associated with the spin-orbit interaction strength, we fit ΔG using a one-dimensional disorder model [3], which is frequently used in nanowire FETs. The fitting formula is given as below,

$$\Delta G = -\frac{2e^2}{hL_g} \left[\frac{3}{2} \left(\frac{1}{l_\phi^2} + \frac{4}{3l_{so}^2} + \frac{W^2}{3l_B^4} \right)^{-1/2} - \frac{1}{2} \left(\frac{1}{l_\phi^2} + \frac{W^2}{3l_B^4} \right)^{-1/2} \right]. \quad (1)$$

Here e is electron charge, h is Planck constant, L_g is the gate length, l_ϕ is the phase relaxation length, l_{so} is the spin-orbit length, l_B is the magnetic length given by $l_B = \sqrt{\hbar / (2\pi eB)}$, and W is the nanowire diameter. In this model, we need only two fitting parameters of l_{so} and l_ϕ .

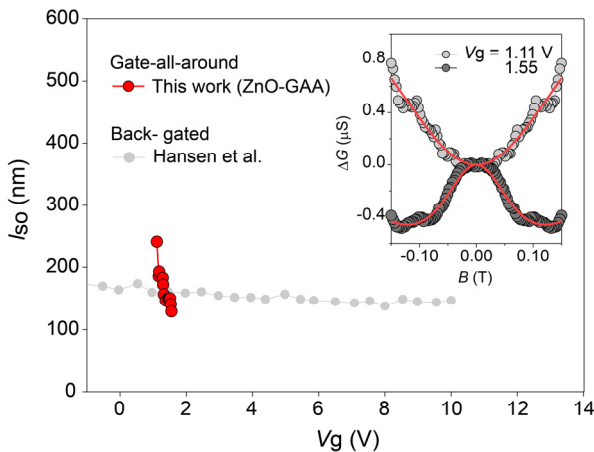


Fig. 2 The spin-orbit length as a function of V_g for our device and previously reported InAs nanowire back-gated MOSFET. The inset shows magnetoconductance as a function of magnetic field obtained with different V_g .

Figure 2 shows l_{so} plotted as a function of V_g for our device and for typical InAs nanowire back-gated FET that is previously reported [3]. We find that our device shows a sharp change in l_{so} with respect to small V_g change at low gate bias, while the conventional back-gated FET shows nearly flat change in l_{so} vs V_g even when the large gate bias is applied. This demonstrates that our GAA MOSFET using conductive ZnO has high gate efficiency for the electrical control of the spin-orbit interaction. While not shown here, these results are comparable to our previous GAA MOSFET using only pure metal, which shows higher gate efficiency than not only conventional nanowire FETs but also previously reported Schottky FETs fabricated from two-dimensional quantum well using InGaAs [7] and InAs [8]. We finally note that, very recently, several models have been published to describe and estimate the Rashba spin-orbit interaction with different calculation techniques. Therefore, in the conference, we will mention analysis using other models, but owing to our calculation along with recently reported new models, the high gate efficiency itself and the advantage for our device structure stay the same.

3. Conclusions

We report electrical characterization of an InAs nanowire FET with a gate-all-around structure using all ALD-grown $\text{Al}_2\text{O}_3/\text{ZnO}$ gate-stack. We demonstrate that this type of device significantly changes the spin-orbit interaction with a small gate bias. This will contribute to a prototype of low-power consumption spin-orbitronics device that can be combined with unique optical properties of ZnO in future optoelectrical hybrid devices.

Acknowledgements

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