Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp619-620

CMOS Compatible Josephson Junctions for Superconducting Qubit Applications

Ts. Ivanov[1], A. Potocnik[1], D. Wan[1], J. Verjauw[1,2], J. Jussot[1], M. Mongillo[1], R. Acharya[1,2], F. A. Mohiyaddin[1], P. Favia[1], H. Bender[1], L. Goux[1], B. Govoreanu[1], and I. P. Radu[1]

[1] IMEC vzw Kapeldreef 75, B-3001 Leuven, Belgium; [2]KULeuven, Kasteelpark Arenberg 10, 3001 Heverlee, Belgium;
Phone: +3216283603 E-mail: Ivanov.Tsvetan@imec.be

Abstract

An industry compatible Josephson Junction (JJ) fabrication process for superconducting qubit applications has been developed. Special attention is given to the main challenges and their solutions. Electrical data of JJs and qubits at room- and cryo- temperatures is coupled with physical analysis to gain insight on how to improve the junction and qubit performance.

1. Introduction

State-of-the-art superconducting qubits based on JJs are fabricated with shadow evaporation technique [1,2]. While this is a convenient process for small scale experiments, the technique yields large variation, low reproducibility and is not industry compatible for a largescale quantum computer. Devices with normal-angle evaporation and Ar plasma clean steps have been reported [3,4], but they are also based on lift-off process and suffer from poor JJ area control.

This work describes a fully CMOS compatible dry etch JJ fabrication process, validated by superconducting qubit demonstration.

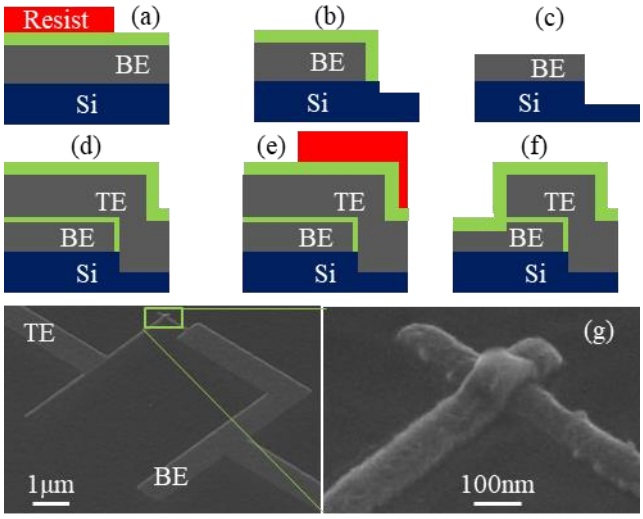

Fig.1. (a) BE deposition and lithography, (b) BE dry etch; (c) Ar sputtering of AlO_x native oxide (d) in-situ controlled oxidation and TE deposition; (e) TE lithography; (f) final JJ; (g) tilted SEM of a single JJ test structure with nominal area 0.01μm^2.

2. Fabrication process and challenges

The key process steps are illustrated in Fig.1. The qubit fabrication starts in the IMEC pilot line, where a readout resonator is patterned out of a 100nm thick Nb layer, deposited on a standard Si wafer. The diced samples receive a solvent and O_2 plasma clean, before loading in the Pfeiffer Spider 630 sputter system. For both Bottom and Top Electrodes (BE/TE) of the JJ, 50nm Al layers are deposited and patterned in F7000S-Advantest e-beam system with ma-N2400 series negative tone resist. The Al is etched in an Oxford Plasmalab 100 ICP dry etching system with $SiCl_4$ chemistry. Cl-based etching of Al is known to cause incorporation of by-products in the resist, forming a resilient crust, and responsible for post strip corrosion. Since BE morphology is detrimental for the JJ quality [5], the resist stripping strategy plays a major role. Standard solvent treatment based on Acetone/IPA is usually insufficient. As evident from Fig.1g, a good result is obtained in combination with wet (EKC265) and dry (O_2 plasma) strip.

The native AlO_x of the BE is removed by physical Ar sputtering in the load lock of the deposition tool. The sample is mounted on Si pocket wafer to avoid JJ contamination with resputtered material from the chuck. To evaluate the effectiveness of AlO_x removal, a series of samples are fabricated with different sputtering power/duration (without controlled oxidation), until the resistance of the test structures became equal to the resistance of the leads (~100Ω). This is the SHORT data point denoted in Fig.3.

The next step is controlled oxidation, during which both the pure O_2 flow and pressure were kept constant, while the load lock is continuously evacuated. For the electrical data reported in Fig.3, only the oxidation duration is varied. The pressure is kept at the highest possible value in the tool to improve AlO_x composition and reduce process variation [6].

The TE dry etch step must be carefully tuned in combination with BE initial thickness optimization, because of the BE consumption during the TE overetch. For thick (≥100nm) BE, careful control of the etch directionality is required, to avoid parasitic junction formation at the BE sidewall. For thin (<100nm) BEs, the Ar sputtering provides sufficient thinning of the BE edge (rounding), mitigating this issue. However, this puts an upper limit on the TE overetch.

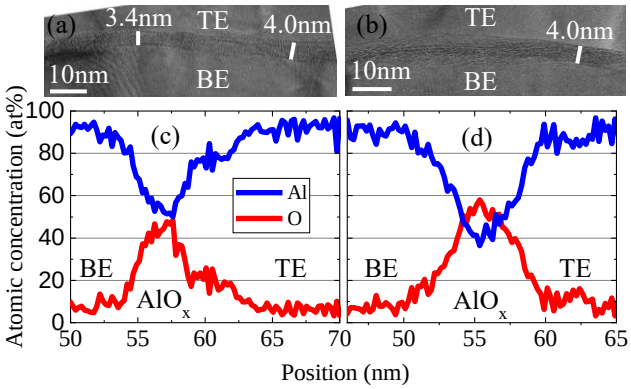

Fig. 2. TEM and elemental profiles (EDS) across JJs formed with (a), (c) 2min and (b), (d) 5 min controlled oxidation.

3. Physical analysis

Cross sectional transmission electron microscopy (TEM) and energy dispersive spectroscopy (EDS) of a set of samples with different oxidation conditions are presented in Fig.2. The measured physical thickness of both AlO_x layers is similar, but there is a clear difference in Al/O elemental ratio. This hints that structural changes are possible even after the self-limiting thickness of the AlO_x layer is reached, contrary to the assumption in [6].

4. Electrical analysis

Room temperature data – From the linear part of the IV characteristic around 0V, the resistance of 27 or 54 identical single JJs is extracted, for 21 nominal JJ areas in the range 0.01-0.18 μm^2. The resistance-area product (RA) as a function of oxidation duration (at constant pressure) is well fitted with a power function and the obtained exponent of 0.45±0.02 is in a good agreement with the empirical formulas reported in [3,7] (see Fig.3). Sample to sample variation is significant, but the resistance distributions for the most uniform sample has a standard deviation σ <2% (inset of Fig.3). The origin of this variation are the physical native oxide removal plus controlled oxidation steps, line edge and Si substrate roughness.

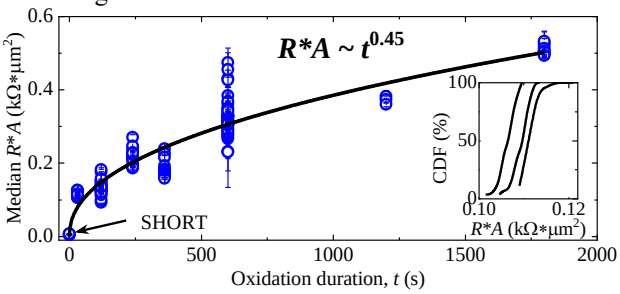

Fig. 3. *RA* product vs. oxidation duration. Inset: Cumulative distribution for 3 JJ areas from *t*=30s sample with σ <2%.

Low temperature data –JJs are tested as qubits at deep cryogenic temperatures (~10mK). Two JJs forming a SQUID are combined with superconducting coplanar capacitor to form a Transmon qubit [8]. This is a building block of superconducting quantum computers [9]. The qubit and a corresponding readout (RO) resonator are integrated on a silicon chip equipped with coplanar waveguide feedlines. Fabricated devices are packaged in high-purity copper sample holders and placed in a dilution refrigerator together with cryo-perm magnetic shielding. Input lines connecting room-temperature electronics and the sample at base temperature are heavily attenuated to minimize thermal radiation reaching the device from warm stages of the refrigerator. Weak output signals are filtered and amplified both with cryo and room temperature amplifiers. Microwave pulse generation and detection is achieved with the Keysight quantum engineering toolbox. The qubits are characterized by excitation with a 48 ns (π pulse) or 24 ns (π/2 pulse) long microwave pulses at 8 GHz and reading the state of a qubit by measuring the phase of the reflected microwave signal from the readout resonator at 6.4 GHz. Using T_1 and T_2^* pulse sequences (see Fig.4) we obtained relaxation time T_1 = 0.81±0.05 μs and decoherence time T_2^* = 0.80±0.12 μs. The above measurements demonstrate that the JJ fabrication process described in Section 2 can successfully build superconducting qubits. Although the relaxation and coherence times are not yet at the state-of-the-art values, they are very promising, considering that the process is in its early stages of development and is fully compatible with CMOS-technology requirements.

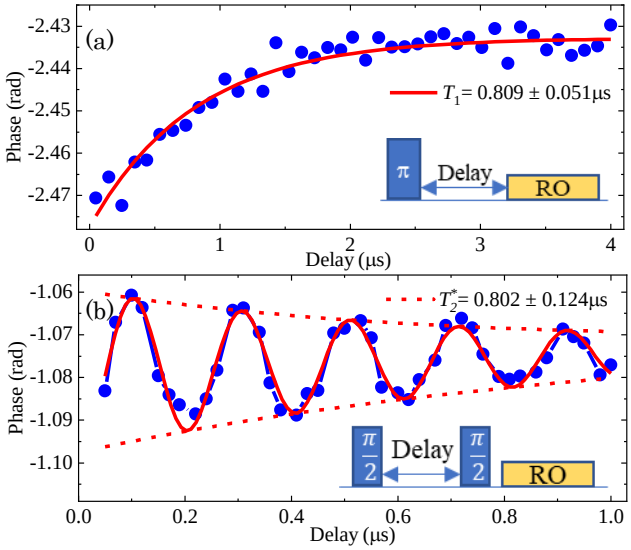

Fig. 4. Qubit relaxation time T_1 (a) and coherence times T_2^* (b) measurements. The pulse scheme used to perform these characterizations is depicted in the inset.

Methods to improve qubit performance – Participation-ratio simulations suggest that a significant fraction of the electromagnetic energy is present in the substrate and native oxides, which contributes to losses in the vicinity of the JJ. Therefore, a high resistivity Si substrate is crucial for long qubit coherence times. The contribution of the native oxide can be reduced by Si recess at the sides of the junction [10]. Reduction of the line edge and surface roughness of the BE, by tuning the Al deposition and Ar sputtering parameters are also beneficial.

5. Conclusions

A versatile JJ fabrication process is developed with industry compatible techniques. The duration of the oxidation step, alters the Al/O elemental ratio in the AlO_x layer, controlling the JJ resistance. The demonstrated superconducting qubit, built with this process, opens up a path for future applications.

Acknowledgements This work is funded by IMEC's industrial affiliation program on Quantum Computing.

References

[1] G. J. Dolan, Appl. Phys. Lett. **31** (1977) 337.
[2] A. Potts, *et al.*, J. Mater. Sci.: Mater. Electron. **12** (2001) 289.
[3] X. Wu, *et al.*, Appl. Phys. Lett. **111** (2017) 032602.
[4] P. Winkel, *et al.*, arXiv:1909.08037v2 (2019).
[5] S. Fritz, *et al.*, Sci. Rep. **8**(1) (2018) 7956.
[6] S. Fritz, *et al.*, arXiv:1910.12963 (2019).
[7] L. J. Zeng, *et al.*, J. Phys. D: Appl. Phys. **48** (2015) 395308.
[8] J. Koch, *et al.*, Phys. Rev. A **76** (2007) 042319.
[9] Y. Tabuchi, *et al.*, IEICE Trans. Electron. **E102–C**(3) (2019) 212.
[10] Y. Chu, *et al.*, Appl. Phys. Lett. **109** (2016) 112601.