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Fabrication and Room Temperature Characterization of Trilayer Junctions for the Development of 300 mm Compatible Superconducting Qubits

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Abstract

We present the development of trilayer-based superconducting qubits fabricated in imec's 300 mm pilot line. Josephson Junctions (JJs) made from Nb/Al-AlO$_x$/Nb trilayer stacks were fabricated and tested at room temperature paying special attention to thermal stability of the stack. The room temperature electrical results obtained on over 20,000 JJs show high yield, excellent resistance targeting, and low variability ~1% on 300 mm wafers.

1. Introduction

Current implementations of superconducting quantum computers require the fabrication of numerous coupled qubits with predictable transition frequencies and long coherence lifetimes. Time-varying fluctuations and reproducibility remain major challenges to this goal and illustrate the need for improved process control in qubit manufacturing. Shadow evaporation has recently shown significant progress in terms of device variability [1] but this technique is not fully compatible with the conventional CMOS fabrication environment. A trilayer based approach [2] on the other hand is compatible. Trilayer qubit fabrication can leverage state-of-the-art production tools and processing techniques only available on 300 mm platforms, providing a potentially viable path towards scalable, fault tolerant quantum computing.

In this work, we fabricate tens of thousands of JJs per 300 mm wafer and perform room temperature characterization on them. Normally, cryogenic measurements of individual JJs on this scale is prohibitive due to the expense and time investment. It is however very well established that the critical current of a JJ and its normal state conductance are related. That is, precise control of the room temperature resistance and variability of JJs directly correlates to precise qubit frequency and frequency variations [2]. Therefore, we focus on room temperature testing of JJs to characterize and minimize their variability.

2. Device Fabrication and Integration

Figure 1 outlines the key process steps for the fabrication of trilayer-based superconducting qubits. In this work, Nb/Al-AlO$_x$/Nb stacks (Fig. 1a) are deposited in-situ using DC magnetron sputtering in a 300 mm cluster system at room temperature with base pressure below 10^{-5} Pa. AlO$_x$ is formed via in-situ thermal oxidation. Using 248 nm DUV lithography and reactive ion etching, the pillar is first patterned in the TE layer to define the JJ (Fig. 1b). Resonators, coupling capacitors, and other structures are then patterned into the BE layer (Fig. 1c). Next, structures receive oxide gapfill and CMP for planarization (Fig. 1d). Finally, continuity between the top of the pillar and BE layer is made by employing oxide via patterning (Fig. 1e), Nb gapfill, and finally subtractive etch of Nb (Fig. 1f) to complete the trilayer qubit.

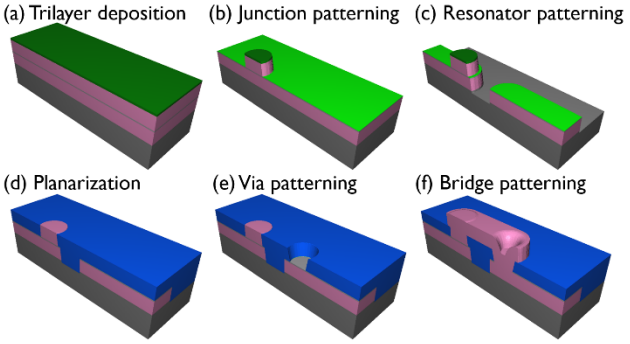

Fig. 1. a-f) Trilayer based superconducting qubit process modules.

This process was applied on 300 mm wafers yielding in the fabrication of X-mon and Transmon qubits, and > 80k JJs per wafer (Fig. 2a). A schematic and TEM cross-section of a completed JJ and via are shown in Fig. 2b-c. Since vias have resistance of only ~1 ohm, we focus on 4-probe measurements of JJs in the cross-bridge Kelvin resistor (CBKR) geometry pictured in Fig. 2d-e.

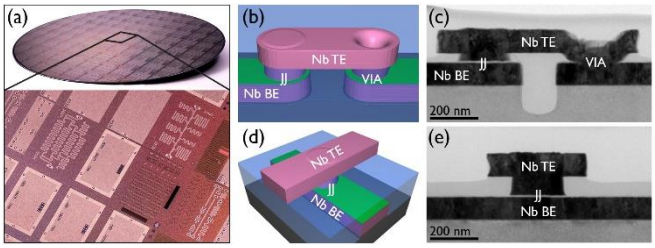

Fig. 2. a) Photograph of a 300 mm wafer with completed trilayer fabrication process, b-c) schematic and TEM cross-section of a JJ and via, d-e) CBKR schematic and TEM cross-section of a single JJ.

Initial JJ testing revealed that process temperature must be carefully controlled during fabrication. Indeed, Nb is known to be sensitive to room temperature oxidation, diffusion, and intermixing. Limiting thermal budget can help minimize environmental impact on Nb-based trilayer stacks. Figure 3 shows TEM and EDS close ups and line scans of the

junction for 2 different wafers. Figures 3a-d show the as-deposited stack and Figs. 3e-h show a stack that has seen high temperature (HT) processing (≤ 300˚C). AlO_x is only present at the top interface for the as-deposited stack (Fig. 3c-d) as intended, but the cross-section of the HT wafer clearly shows a second barrier formed at the Nb-Al interface (Fig. 3g-h). The line scan in Fig. 3h also shows an increase in atomic concentration of O suggesting oxygen diffusion and intermixing at the Nb-Al interface.

A comparison between JJs fabricated using a lower temperature (LT) process (≤ 205˚C) and the HT process is shown in Fig. 3i. The resistance-area product (RA) has been plotted showing very wide distribution for the HT process, but RA greatly improves and has very narrow distribution for the LT process demonstrating the need to control for thermal budget of Nb trilayer stacks. All remaining results in this abstract were obtained on junctions processed using the LT process.

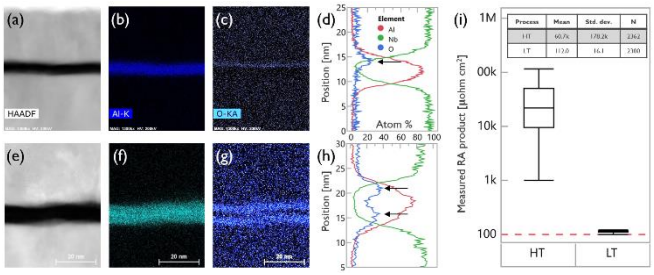

Fig. 3. (a-h) HAADF, EDS, and line scans showing single and double barrier (arrows) for as-deposited and HT trilayers, (i) RA comparison for LT vs HT processes. Red dotted line is the target RA.

3. Results and Discussion

Precise control of JJ critical current, which is directly related to the normal state resistance, is crucial for engineering qubits with high accuracy in frequency. Using the Current-In-Plane Tunneling (CIPT) method to measure RA of as-deposited trilayer stacks, we employ varying methods of junction oxidation and parameters and demonstrate the ability to sample a large range of RA values (Fig. 4a) at blanket level.

Wafers with a known blanket RA value are then processed using the full qubit flow and tested to compare with measured RA from JJs. Fig. 4b shows distributions of thousands of measured JJs showing that the measured RA is very close to target RA at blanket and that there is minimal impact due to processing. The relative standard deviation (RSD) is on the order of a few % indicating very small RA variability possibly due to barrier pinholes or inhomogeneities.

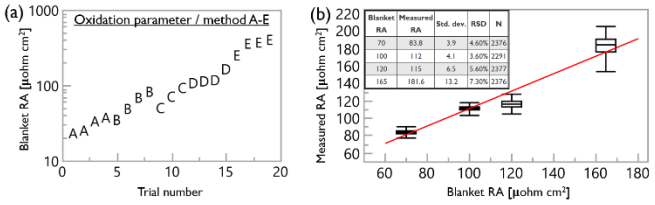

Fig. 4. (a) Blanket RA obtained from CIPT on wafers with varying oxidation parameters and methods, (b) measured RA vs blanket RA. Inset shows < 10% variability. The red line is a guide for the eye.

To quantify the impact of processing on yield and device variability, JJs with nominal CDs ranging from 200 nm to 1200 nm were fabricated and tested. Resistances were acquired for each CD (Fig. 5a) with nearly 100% yield (Fig. 5b) and found to be close to expected values based on nominal CD and blanket RA. Resistances were off by ~10% attributed to process variations. The 200 nm structure performed the worst possibly due to the limitation of 248 nm lithography at scaled dimensions. RSD is plotted in Fig. 5c for each structure showing exceptionally low resistance variability ~1% for the largest CDs. This performance surpasses the current state-of-the-art for shadow evaporated JJs [1].

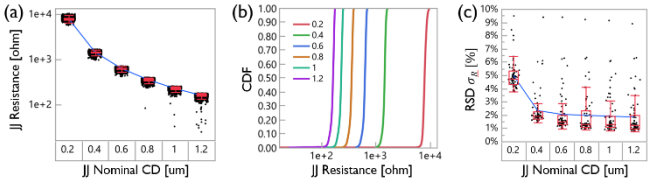

Fig. 5. (a) Resistance, (b) CDF plot, and (c) RSD for all structures.

Examining only the 1um structure with full wafer map and increased JJ sampling, there is a clear radial dependence of the measured resistance along the wafer (Fig. 6a) where JJ resistance at the edge (E) dies is up to 30% lower than at the center (C). RDS map in Fig. 6b shows a similar signature with greatest variability at E. Indeed, CDSEM inspection (Fig. 6c) reveals a consistent C to E non-uniformity where measured JJ CDs are up to 10% larger at E. This increase in JJ area leads to a proportional decrease in JJ resistance for the E dies.

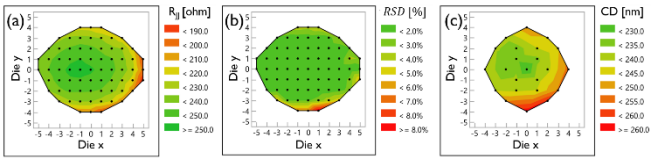

Fig. 6. (a) Resistance wafermap and (b) RSD wafermap for 1 um CD JJ, and (c) CDSEM map for 200 nm JJ

3. Conclusions

We have fabricated Nb-based trilayer superconducting qubits using a full 300 mm process on production capable tools. Room temperature resistance of many thousands of JJs was measured showing good match between blanket RA and RA of processed wafers with exceptionally low resistance variability down to 1%. This result is expected to translate to reduced qubit device variability and improved predictability of qubit transition frequencies at cryogenic temperatures, which is key for future quantum computing devices.

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