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Readout of Charge States in a Physically Defined PMOS Silicon Quantum Dot via RF Reflectometry

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Abstract

In this study, we have embedded a physically defined p-channel Si-MOS quantum dot (QD) device into an impedance transformer LC circuit. We reduce the top gate area of the device down to 300 nm square to decrease the parasitic capacitance, which causes low-bandwidth and prevents the RF signal to reach QD. We show that it is possible to perform readout of charge states at 4.2 K by RF reflectometry.

1. Introduction

Quantum information processing based on silicon QDs is an appropriate platform for quantum computers thanks to its long coherence time [1] and its compatibility with CMOS technology [2-3]. Particularly PMOS silicon QDs are convincing for the development of a spin-based qubit system since hole spins have smaller hyperfine interactions than that of electron spins and can be controlled only with an electric field as they have strong spin-orbit coupling (SOC) [4-6].

Charge sensing technique, in which a capacitively coupled additional single QD (SQD) is required, has been used extensively to map out the charge states in QDs. While this technique is relatively easy to demonstrate, the integration time (t_{min}), which is the minimum time to discern and characterize the states, should also be considered. For a readout to be effective, the measurement needs to be faster than the relaxation time of the system. In quantum computing, in order to perform error correction the measurement time should be faster than the coherence time ($T_2{}^*$). For silicon qubits, t_{min} should be lower than 20 us [7].

Measurements done with charge sensing are restricted by the RC time constant of the charge sensor. Usually, these numbers are $R > 50$ kΩ and C in the order of hundreds of pF that inhibit a charge sensor bandwidth to a few kilohertz or less [8]. Instead of performing a standard voltage and current tests, DC measurement, a so-called RF single electron transistor (RF-SET) overcomes the low-frequency restriction by using an LC-resonant tank circuit to measure RF waves, which are reflected from the SET.

2. Device fabrication

A scanning electron microscope (SEM) image and schematic of physically defined PMOS double QD (DQD) and SQD on undoped silicon-on-insulator (SOI) substrate are shown in Fig. 1(a), and 1(b), respectively. The dark and bright regions in Fig. 1(a) indicates the BOX layer of the-structure, and the SOI layer, respectively. The devices have three side-gates (G_l, G_m, G_r) capacitively coupled to DQD and one side gate (G_{sqd}) capacitively coupled to SQD for controlling electrochemical potential. A 300-nm-square area on the QDs is covered with poly-Si to form the top gate. Buried oxide has a thickness of 135 nm, and gate oxide has a thickness of 65 nm. Channels out of the top gate are doped with boron at the dose of 1.0 x 10^{-20} cm^{-3}. When a negative voltage, V_{TG}, is applied to the top gate, holes are induced in the QDs. In this measurement, for simplicity, we used only an SQD.

3. Method and discussion

In this study, we use the RF-SET technique to readout charge states in a physically defined PMOS silicon QD device whose top gate area is reduced down to 300 nm square to fully overcome low-pass filter problems that exist in MOS devices with top gate area of a few μm squares [9]. We first find the resonant frequency of the device when bonding wire is connected to the drain lead of SQD mounted on an FR4 printed circuit board (PCB). Using a 2.2 μH commercial inductor in a series LC resonant tank circuit (Fig. 2(a)) gives us a resonant frequency of 210.875 MHz from which we found the parasitic capacitance (C_p) as 0.258 pF by using Eq. (1).

$$f_r = \frac{1}{2\pi\sqrt{LC_p}} \qquad (1)$$

This value is much lower than that obtained for the device with 10-um-square top gate, 0.6 pF, as we expected [9]. We then send 210.875 MHz carrier frequency in the time domain to the SQD through drain lead. Before the signal reaches the sample, we attenuated with an -40 dB attenuator to avoid blowing up the device. Electron transition through SQD causes a change in amplitude of the reflected signal. The directional coupler sends the carrier signal down one line, and the reflected signal up another line. The reflected the reflected signal is transmitted through the directional coupler back up the carrier line. Afterward, the signal is amplified with room temperature amplifiers, which has a gain of 60 dB in total.

Amplitude change in reflected signal was mapped out by sweeping the top gate voltage and analyzing S parameters as shown in the lower panel of Fig. 3(a). At the same time, we performed standard I-V measurement as shown in the upper panel of Fig. 3(a). Following, we performed a similar measurement by sweeping the side gate voltage while applying a

constant negative voltage to the top gate to create a channel between source and drain (Fig. 3(b). Coulomb peak characteristics are the same in both DC and RF measurements, meaning that we succeeded in the readout of charge states via RF-SET technique with improved device structure.

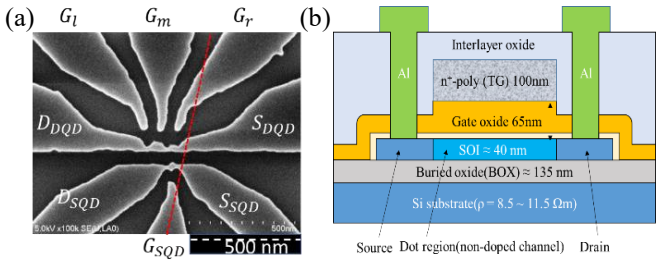

Fig. 1 Physically defined p-channel Si-MOS device. (a) Scanning electron microscope image of the device. (b) Cross-sectional schematic of the device structure along red dashed line in (a).

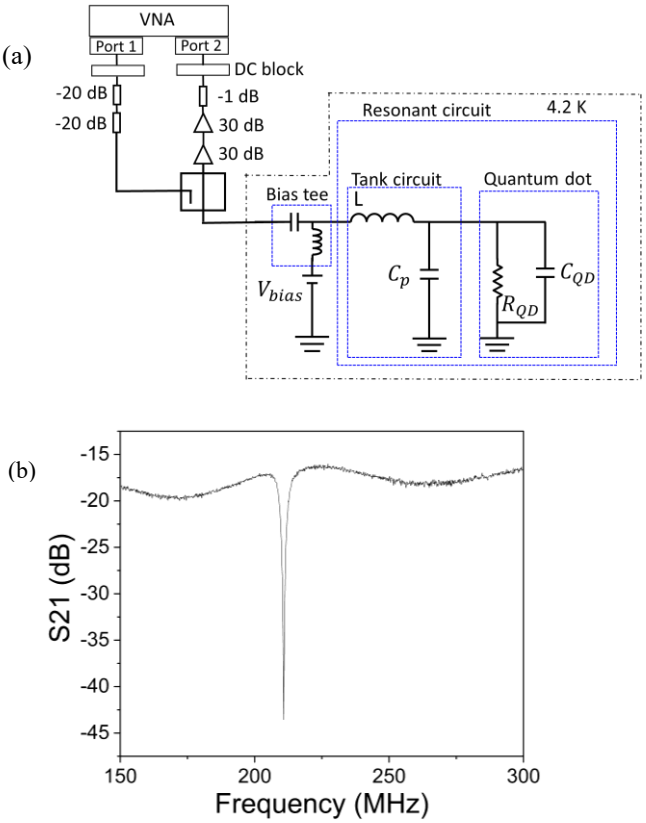

Fig. 2 (a) Measurement setup. Attenuated RF signal is sent through Series LC resonant tank circuit to drain of single quantum dot (SQD) and reflected signal that is separated by directional coupler is amplified at room temperature before it reaches the second port of vectoral network analyzer. (b) S21 as a function of frequency. Resonant frequency, $f_r = 210.875$ MHz, of the sample is shown when top gate voltage is not applied

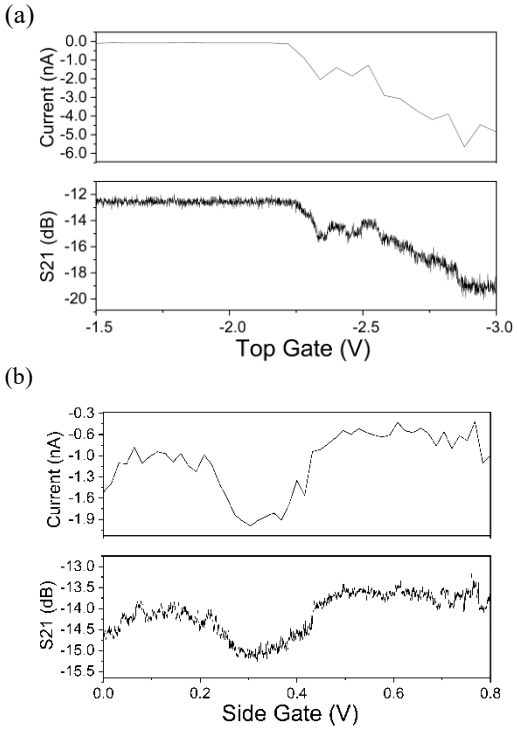

Fig. 3 Time-dependent RF and DC measurements with sweeping top gate (a) and side gate with constant top gate voltage, $V_{TG} = -2.5\,V$ (b).

4.Conclusions

We have fabricated physically-defined PMOS QDs with smaller top gate area and performed RF-SET measurements. We observed the Coulomb peaks via RF, and this result is in good agreement with what we obtained with standard DC measurement. This result shows us a route to spin readout in our future work.

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References

[1] M. Veldhorst et al., Nature 526, 410-414 (2015).
[2] B. M. Maune et al., Nature 481, 344–347 (2012).
[3] K. Takeda, et al., Science Advanced, 2, 8, 1600694-1-6(2016)
[4] B. Voisin., et al., Nano Lett., 16 (1), 88-92 (2015).
[5] Li. Ruoyu., et al., Nano Lett., 15.11 (2015).
[6] R. Maurand, et al., Nat. Commun. 7 13575 (2016).
[7] R. Leon, et al., Nat. Commun. 11, 1 (2020)
[8] M. Manoharan et al., Nano Lett. 8 (12), 4648-4652 (2008).
[9] Y. Yamaoka et al., Jpn. J. Appl. Phys. 56, 04CK07 (2017).