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High-Performance Source-Follower-Based ITZO TFT Circuits for Organic Active Pixel Image Sensors

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Abstract

We discuss an active pixel sensor (APS) readout circuit based on indium-tin-zinc-oxide thin-film transistors (TFTs) for three-stacked organic image sensors. A pixel layout of the APS was designed using three TFTs with a channel length of 2 µm, and its performance was experimentally evaluated by fabricating a source follower (SF) circuit with the pixel layout design. We found that the designed APS exhibits high SF voltage gain of ~0.89 with satisfactory linearity achieved in a wide output voltage range.

1. Introduction

Three-stacked organic image sensors comprise single-chip sensors with a structure in which three organic photoconductive films (OPFs) sensitive to the primary colors (blue, green and red) and three thin-film transistor (TFT)-based readout circuits are stacked alternately. They can perform color separation in the vertical direction without the need for color filters or prisms, which are used in conventional single- or three-chip imaging systems, and thus have been studied in expectation of achieving compact single-chip cameras with high utilization efficiency of light comparable to that of three-chip ones. To date, organic image sensors using three OPFs have been fabricated and their color imaging capability has been investigated [1,2]. Moreover, recent advances in pixel-size reduction and high pixelation of TFT circuits have made it possible to fabricate an organic image sensor with a pixel array of 320 × 240 (QVGA) using a single OPF [3]. In the previous studies, however, passive pixel sensor readout circuits with one TFT per pixel were utilized and thus, the reproduced images were susceptible to the effect of external noise.

Here, we propose an active pixel sensor (APS) readout circuit to reduce the noise in three-stacked organic image sensors. A pixel layout of the APS circuit with a pixel pitch of 90 µm was designed using three indium-tin-zinc-oxide (ITZO) TFTs with a channel length of 2 µm, and its performance was experimentally evaluated by fabricating a source follower (SF) circuit with the designed pixel layout.

2. Design and Simulation of the ITZO-TFT-Based APS

We first designed a prototype QVGA APS circuit using ITZO TFTs having a channel length of 2 µm and a channel width of 10 µm. Figure 1(a) shows the schematic circuit diagram of our quasi-QVGA APS circuit. The APS circuit consists of a pixel circuit, a vertical signal line (VSL), a TFT used as a load transistor (M_L), a correlated double sampling (CDS) circuit (added as an external readout circuit) and delay equivalent circuits of the QVGA pixel array. Figure 1(b) shows the schematic diagram of the pixel circuit. The pixel circuit was designed on the basis of the results of a simulation of an ITZO TFT APS reported in the literature as a benchmark for SF circuit performance [4]. The designed pixel circuit possesses three TFTs used as select, amplifier and reset transistors (M_S, M_A and M_R), and an OPF on a pixel electrode, which generates a signal charge under light irradiation. The SF amplifier comprises M_A and M_L and amplifies the signal charge. In the operation of the APS, charge accumulation, pixel signal readout and reset signal readout are performed in this order with gate pulses of M_R (V_{RG}) and M_S (V_{SG}) under applied drain bias voltages of M_A (V_{DD}) and M_R (V_{RD}) with a gate bias voltage of M_L (V_{LG}).

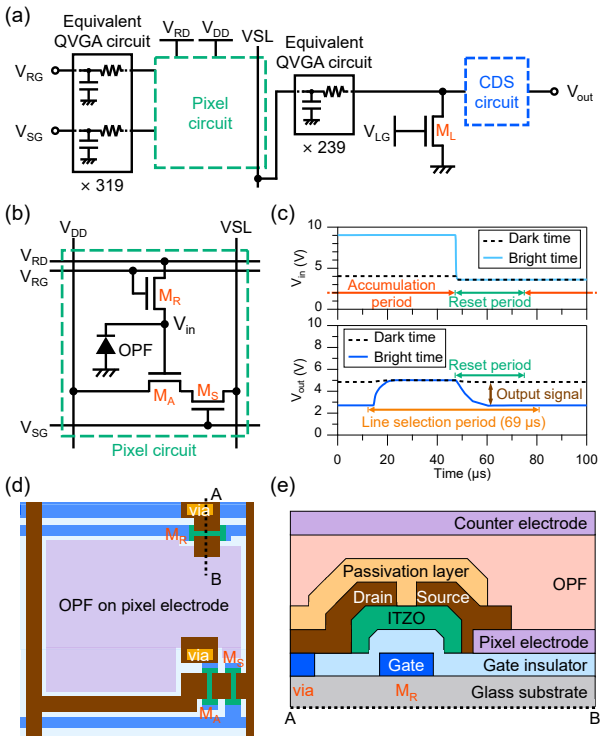

Fig. 1 (a) Schematic diagram of our quasi-QVGA APS circuit containing a CDS circuit. (b) Schematic diagram of the pixel circuit. (c) Simulational input (top) and output (bottom) characteristics of the designed APS circuit. (d) Schematic of the designed layout of the pixel circuit. (e) Typical cross-sectional schematic of the designed pixel circuit along the line A–B marked in (d).

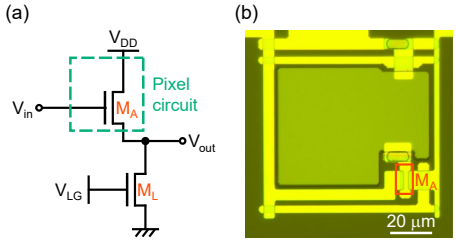

Fig. 2 (a) Schematic diagram of the SF circuit. (b) Optical microscope image of the pixel circuit containing M_A.

Figure 1(c) presents the input (V_{in}) and output (V_{out}) characteristics of the designed APS circuit obtained by circuit simulation using the TFT model based on experimental data. The correspondence between V_{in} and V_{out} can be observed, and the APS operation was found to be completed within the line selection period (69 μs for 60 fps, QVGA).

Figure 1(d) shows the schematic of the designed pixel circuit layout. It has a pixel size of 90 μm and an opening ratio of ~47%, which was determined so that the opening area is comparable to that reported in the literature [4]. Figure 1(e) shows a typical cross-sectional schematic of the designed pixel circuit along the line A–B marked in Fig. 1(d). The entire circuit is based on TFTs with a bottom-gate back-channel etched structure, and via holes are placed to connect the gate and source drain electrodes.

3. Fabrication and Characterization of the SF Circuit

To evaluate the performance of the designed APS circuit, we next fabricated an SF circuit composed of M_A in the pixel layout and M_L, as shown by the equivalent circuit in Fig. 2(a). Gate electrodes were formed with a 50-nm-thick molybdenum (Mo) alloy, and then a silicon oxide (SiO_x) gate insulator with a thickness of 200 nm was deposited by sputtering. A 50-nm-thick indium-tin-oxide (ITO) layer was then deposited as a pixel electrode, and a semiconductor layer of 30-nm-thick ITZO was formed by sputtering. Via holes were then generated by reactive ion etching, and source drain electrodes were formed with 70-nm-thick Mo alloy. An organic insulator with a thickness of 600 nm was then spin-coated as a passivation layer.

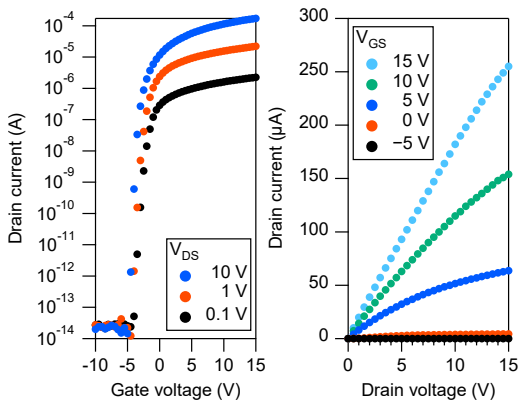

Fig. 3 Typical transfer (left) and output (right) characteristics of the TFT in the fabricated SF circuit.

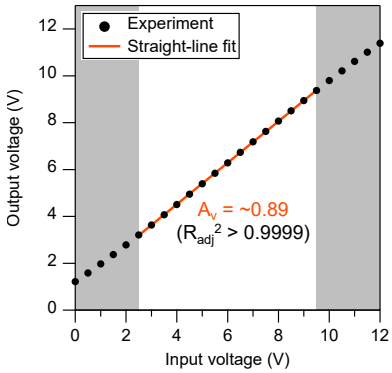

Fig. 4 Experimental input–output characteristic of the SF circuit (black) and its straight-line fit (red) applied in the nonshaded region.

Figure 2(b) shows an optical microscope image of the fabricated pixel circuit. The pixel circuit excluding M_S and M_R was successfully fabricated in accordance with its design shown in Fig. 1(d). The TFT characteristics and SF performance of the fabricated circuit were measured using a semiconductor device parameter analyzer (Keysight, B1500A). Figure 3 shows typical transfer and output characterics of the TFT in the fabricated SF circuit. The on–off ratio was found to be $>10^8$ for V_{DS} = 1 V and the field-effect mobility at V_{DS} = 10 V was ~24 cm^2/Vs.

The black circles in Fig. 4 show the experimentally obtained input–output characteristic of the SF circuit at V_{DD} = 15 V and V_{LG} = 1 V. To evaluate the SF performance, a straight-line fit was performed in the V_{in} range from 2.5 to 9.5 V, as shown by the red line in Fig. 4. It was found that voltage gain (A_v) of the SF circuit is ~0.89 (determined from the gradient of the line) and the adjusted R-squared value (R_{adj}^2) is > 0.9999 with a V_{out} range of ~6.2 V. These values are higher than the simulation-based ones previously reported [4], despite the use of more miniaturized ITZO TFTs, and the designed APS circuit was found, from this result, to exhibit excellent SF performance with satisfactory linearlity.

4. Conclusions

We designed an APS circuit with a pixel size of 90 μm using ITZO TFTs with a channel length of 2 μm, and its performance was evaluated by fabricating an SF circuit with the pixel layout design. The designed APS circuit was found to exhibit high SF voltage gain of ~0.89 acheved in the output voltage range of ~6.2 V with satisfactory linearity. In the near future, the dynamic response characteristics of the designed APS circuit will also be evaluated.

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