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Suppression of Channel Shortening and Reduction of S/D Parasitic Resistance in InGaZnO channel BEOL Transistor by Insertion of thermally stable InAlZnO Contact Layer

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Abstract

We have demonstrated a suppression of channel shortening and a reduction of S/D parasitic resistance (R_{para}) in InGaZnO (IGZO)-FET after high temperature annealing by inserting InAlZnO (IAZO) contact layer (CL) between S/D electrode and channel. Thanks to high bond dissociation energy of Al with oxygen, tungsten (W) film covered by IAZO maintained a low resistivity during high temperature annealing (>400℃), while W film covered by IGZO significantly increased its resistivity due to the formation of metal oxide interlayer. IGZO-FET with IAZO-CL shows both improvement of V_{th} roll-off and reduction of R_{para} by ~30%, with maintaining high mobility (>15 cm^2/Vs) even after 420ºC annealing in N_2. The insertion of IAZO contact layer is a promising technique to achieve IGZO-channel BEOL transistor with high thermal stability and high on-current.

(Keywords: oxide semiconductor, InGaZnO, InAlZnO)

Introduction

Field-effect-transistor (FET) using oxide semiconductors (OS) as channel layers have attracted much attention as BEOL transistor for 3D-LSI applications such as high voltage I/Os and embedded memory by its high mobility (>10 cm^2/Vs), high breakdown voltage (V_{BD} >40V) and ultralow leakage current (<10^{-22} A/μm) [1-5]. For integrating OS-FET in BEOL of Si CMOS LSI, oxidation/deoxidation between OS channel and S/D electrode during thermal process (> 350ºC) causes two fatal issues especially for scaling beyond 1 μm gate length region as shown in Fig.1 (a) ; (1) a channel shortening caused by extension of N^+ S/D region by the formation of oxygen vacancy (V_o) which generates excess carriers and (2) an increase of S/D parasitic resistance (R_{para}) by the formation of highly resistive oxide interface layer of S/D electrode [6-9]. In order to overcome these issues, we focused on a thermally stable OS material, InAlZnO (IAZO). Since Al-O exhibits much larger bond dissociation energy than Ga-O, IAZO is expected to suppress oxidation/deoxidation with S/D electrode, compared with IGZO [10,11]. We propose an insertion of IAZO as a contact layer (IAZO-CL) between S/D electrode and IGZO channel as shown in Fig. 1(b). In this study, we have successfully demonstrated suppression of channel shortening and R_{para} in IGZO-FET by applying IAZO-CL with maintaining high mobility (>15 cm^2/Vs) of IGZO channel.

Results and Discussion

A. Thermal stability of IAZO-CL

Figure 2 shows four different chemical compositions of IAZO film and their sheet resistances. In Al-rich condition, deposited IAZO film behaved as an insulator. With the decrease of Al composition, the resistivity of IAZO film decreased. Thus, IAZO film in condition 4 (IAZO-4) was expected as a contact layer with low resistivity. Figure 3 shows the O 1s XPS spectra of IAZO and IGZO film. The O1s spectra were deconvoluted into two different peaks, where one is the peak related to metal-O at 530.85 eV and the other is the peak related to oxygen vacancy at 532.10 eV [12, 13]. Smaller peak area in IAZO film indicates Al suppresses V_o formation compared with Ga. In order to investigate the degree of oxidation/deoxidation between S/D electrode and OS channel, the sheet resistance of tungsten (W) film covered by different OS materials were evaluated (Fig.4). The thickness of W and OS film were 10 nm both. In this experiment for IAZO, condition 4 in Fig.2 was used. The resistance of OS/W film corresponded to that of W film during annealing (<380℃). As annealing temperature increases (>400℃), the resistivity of W covered by IGZO was increased drastically, while that of W covered by IAZO was maintained. It suggests that IAZO film suppresses oxidation/deoxidation with S/D electrode (W) and the formation of highly resistive metal oxide interlayer.

B. Characterization of IGZO-FET with IAZO-CL

Figure 5 shows device fabrication process and schematic illustration of IGZO-FET. The thickness of gate insulator, IGZO channel and IAZO-CL were 40 nm, 15 nm and 5 nm, respectively. Tungsten was used as S/D electrodes. Fig. 6 shows I_d-V_g characteristics of IGZO-FET with (w/) and without (w/o) IAZO-CL, after annealing at 420℃ under N_2 atmosphere. *S.S.* value of IGZO-FET w/o IAZO was deteriorated compared with that w/ IAZO-CL. This *S.S.* degradation was due to the shortening of effective channel length in IGZO-FET w/o IAZO-CL. In addition, the increase of drain current by 7% was achieved with IAZO-CL. The comparison of R_{on}-L_g plot in both devices is shown in Fig. 7(a). R_{para} was extracted by the vertical intersection point of R_{on}-L_g plot and extracted R_{para} are shown in Fig. 7(b). R_{para} of IGZO-FET w/ IAZO-CL was confirmed to decrease by 30%, compared with that of IGZO-FET w/o IAZO-CL. This R_{para} reduction is caused by suppression of S/D electrode oxidation by IAZO-CL. Figure 8 shows effective mobility extracted by split *C-V* method. Comparable high mobility (>15 cm^2/Vs) was confirmed in IGZO-FET w/ IAZO-CL. Figure 9 shows the threshold voltage shift (ΔV_{th}) plotted versus L_g, where ΔV_{th} is defined as the difference of V_{th} from V_{th} of L_g =2 μm. IGZO-FET w/ IAZO-CL maintained V_{th} even at shorter L_g (L_g<1 μm), while clear V_{th} drop was observed in IGZO-FET w/o IAZO-CL. This indicates that IAZO-CL has high immunity to deoxidation by S/D metal and suppresses extension of N^+ S/D region toward IGZO channel. Moreover, it was revealed that only 5 nm contact layer played an important role for improving thermal stability of OS-FET without changing the channel material. Figure 10 shows the I_{on}-L_g plot of experimental results and calculated value from extracted mobility and R_{para}. The calculated on-current would increase by 40% at L_g =100 nm w/ IAZO-CL thanks to low R_{para}.

Conclusion

We have successfully demonstrated improvement of thermal stability of IGZO-FET by inserting IAZO contact layer between IGZO channel and S/D electrode. The IAZO contact layer has high immunity to deoxidization of channel by S/D metal and suppresses oxidization of S/D metal during thermal process. By inserting IAZO contact layer to IGZO-FET, V_{th} roll-off was improved and R_{para} was decreased by 30% with maintaining high mobility (>15 cm^2/Vs). These results indicate that IAZO contact layer is promising to realize short channel IGZO-FET for 3D-LSI applications.

References

[1] S. –J. Choi *et al.*, IEICE Electronics Express, 16, 3(2019), [2] K. Nomura *et al.*, Nature, 432,488(2004), [3] K. Kaneko *et al.*, VLSI 2011, p120, [4] T. Aoki *et al.*, ISSCC 2014, p502, [5] S H. Wu *et al.*, VLSI 2016, p58, [6] M. Oota *et al.*, IEDM 2019 p.50, [7] J. Kataoka *et al.*, JJAP, 58, SBBJ03 (2019), [8] K.-H. Choi *et al.*,Appl. Phys. Lett. 102, 052103 (2013), [9] Z. Hu *et al.*, Solid-State Electronics. 104, 39–43(2014), [10] H. Fujiwara *et al.*,VLSI2020, T-H2-2 [11] Y. R. Luo, Handbook of Chemistry and Physics,CRC Press,2007, [12] Jie Zhang *et al.*, J. Vac. Sci. Technol. B 32,1 (2014), [13] Lan Yue *et al.*, J. Phys. D: Appl. Phys. 46,445106(2013)

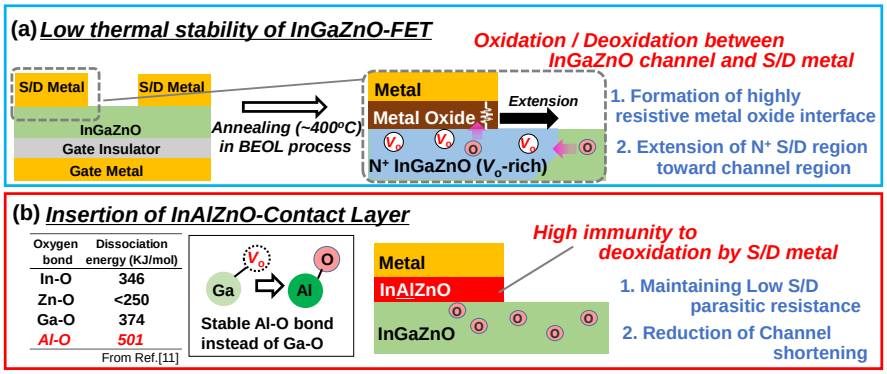
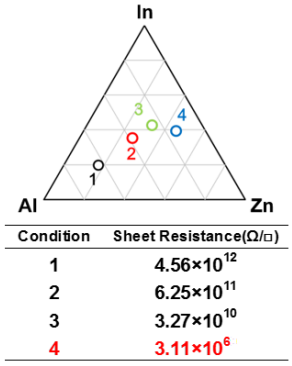


Fig. 1 (a) Schematic illustration of issues in IGZO-channel FET for high-temperature annealing, and (b) list of metal-oxygen bond dissociation energy [11] and concepts of a reduction of S/D parasitic resistance and a suppression of channel shortening by IAZO-contact layer.



Condition	Sheet Resistance(Ω/□)
1	4.56×10^{12}
2	6.25×10^{11}
3	3.27×10^{10}
4	3.11×10^{6}

Fig. 2 Chemical composition and sheet resistance of deposited IAZO films. IAZO film with less Al composition shows a lower resistivity.

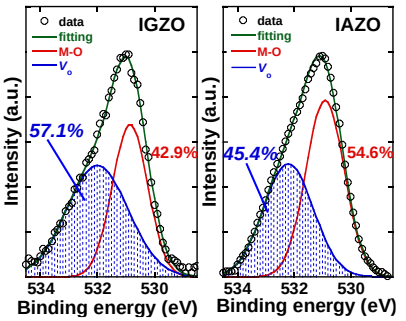


Fig. 3 XPS spectra of O1s in IGZO and IAZO film. The peak area of V_o in IAZO film is smaller than that in IGZO film.

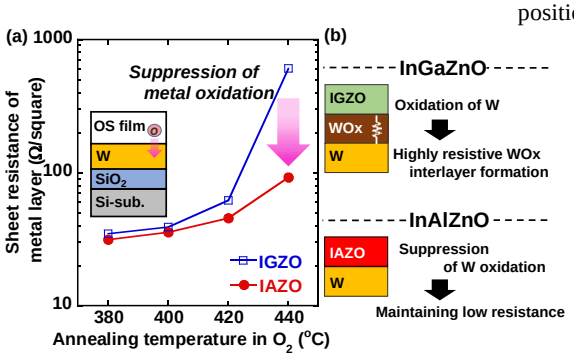


Fig. 4 (a) Annealing temperature dependence of sheet resistance of tungsten film covered by OS materials and (b) schematic diagram of comparison between IGZO and IAZO.

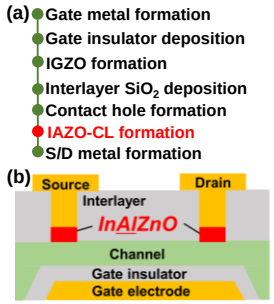


Fig. 5 (a) Fabrication process and (b) schematic image of IGZO-FET w/ IAZO-CL.

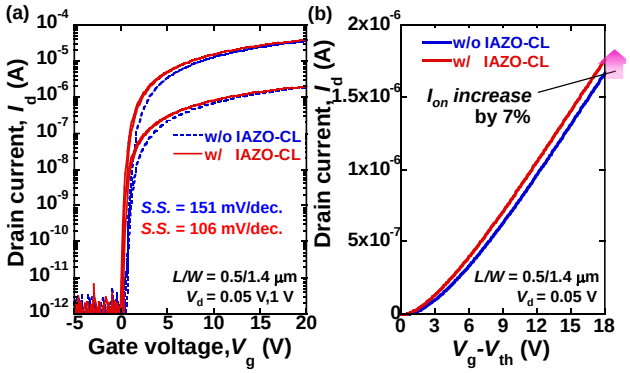


Fig. 6 I_d-V_g characteristics of IGZO-FET w/ and w/o IAZO-CL after annealing at 420°C under N_2 atmosphere. Drain current of IGZO FET w/ IAZO-CL was increased by 7%.

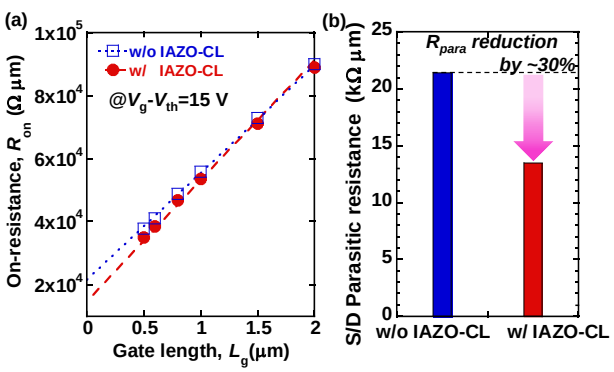


Fig. 7 (a) R_{on}-L_g plot and (b) comparison of R_{para} between IGZO-FET w/ and w/o IAZO-CL. R_{para} is decreased by 30% by the insertion of IAZO-CL.

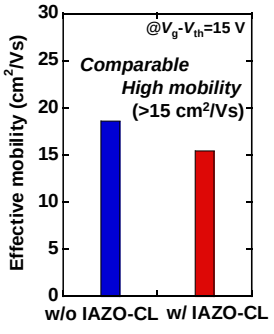


Fig. 8 Effective mobility extracted by split *C-V* method. High mobility (>15 cm^2/Vs) was maintained.

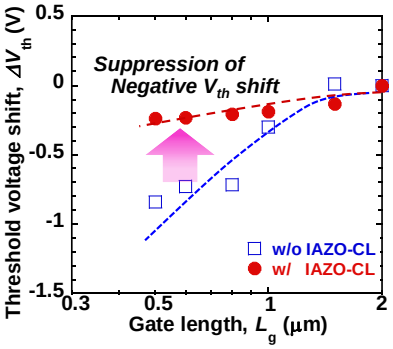


Fig. 9 ΔV_{th} roll-off curve after annealing at 420°C under N_2 atmosphere. Negative shift of V_{th} was reduced by insertion of IAZO-CL.

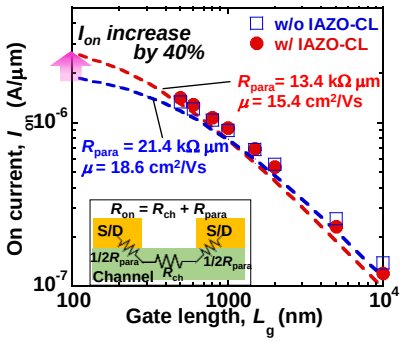


Fig. 10 I_{on} improvement by L_g scaling calculated from extracted mobility and R_{para}. I_{on} is expected to increase by 40% with IAZO-CL at L_g=100 nm.