Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp695-696

Enhanced Electrical Performance and Reliability of Ti-SZTO Thin-Film Transistors with $Hf_{1-x}Si_xO_2$ Gate Dielectrics Using Co-sputtering Technique

Chen-En Lin[1], Shui-Jinn Wang[1, 2*], Rong-Ming Ko[2*]

[1] Institute of Microelectronics, Dept. of Electrical Engineering, National Cheng Kung University, Tainan 701, Taiwan.
[2] College of Electrical Engineering and Computer Science, National Cheng Kung University, Tainan, 701, Taiwan
*Phone: +886-6-2763882 E-mail: sjwang@mail.ncku.edu.tw; ronminko@mail.ncku.edu.tw

Abstract

High performance amorphous Ti-SiZnSnO (SZTO) thin-film transistors (TFTs) with $Hf_{1-x}Si_xO_2$ dielectric layer were fabricated by RF co-sputtering at room temperature. The incorporation of Si in HfO_2 dielectric layer and Ti in SZTO channel layer to reduce the excessive defects in the thin film and improve interface quality to optimize the performances and reliability of devices are demonstrated. Three types of HfO_2/SZTO, $Hf_{1-x}Si_xO_2$/SZTO and $Hf_{1-x}Si_xO_2$/Ti-SZTO bottom gate TFTs were used for comparative analysis. Experimental results reveal that $Hf_{0.82}Si_{0.18}O_2$/Ti(2.5%)-SZTO TFTs exhibit the best device performance with on/off current ratio of 2.78×10^8, threshold voltage of 0.23 V, subthreshold swing of 87 mV/dec, field effect mobility of 36.8 $V^{-1}\cdot s^{-1}$, and interface trapped density of 8.97×10^{11} $cm^{-2}\cdot eV^{-1}$. It also shows the smallest threshold voltage shift after positive/negative bias stress, white light illumination, and thermal stability (at 378 K) tests for 1000 s of 0.103 V/-0.096 V/-0.165 V/-0.105 V. The remarkable improvements should be attributed to the Si incorporation could reduce oxygen vacancies and improve surface roughness of HfO_2 to suppress surface scattering and the amount of charge trapping during the stress test, as well as Ti incorporation reduces defect density in the channel layer.

1. Introduction

Thin film transistors (TFTs) based on amorphous oxide semiconductors, especially amorphous indium gallium zinc oxide (α-IGZO), due to high field-effect mobility, good uniformity, and simple fabrication processes, have been widely used as the core switching elements in large-area flat panel displays. Though wide spread interest have been focused on IGZO TFTs for applications in various fields, IGZO TFTs are liable to incur reliability issue, in addition, since In and Ga are rare metals, they have to face the situations of limited or even constricted supply and high cost. Incorporation of metal ions, such as Hf^{4+}, Si^{4+}, Ta^{4+}, Ti^{4+}, etc. [1] to serve as carrier and oxygen vacancy (V_O) suppressor have been demonstrated. For having higher binding dissociation energy (BDE) of metal to bond with oxygen, they could release the reliability problem and issues caused by rare metal of the IGZO system. Among them, SiZnSnO (α-SZTO) has been shown to be one of choice of channel material in avoiding the use of In and Ga. Basically, Si and Sn is rich in the earth, especially, Sn^{4+} has a large electron orbit $(n-1)d^{10}ns^0$ ($n\geqq4$) similar to In^{3+} that allows high electronic mobility. [2]

To improve TFT performance, the uses of high dielectric constant (high-κ) materials to enhance gate controllability, reduce operating voltage, and leakage current. HfO_2 is one of the most promising high-κ dielectrics with a relative κ value of 25. However, binary HfO_2 usually suffers from high defect density and low poly-crystallization temperature, [3] incorporation of various guest atoms like Si, Al, Ti, etc. to form ternary or quaternary compounds has been shown to improve dielectric quality and increase crystallization temperature.

In this study, incorporation Ti in SZTO channel layer and Si-doped HfO_2 dielectric layer using co-sputtering technique for the fabrication of TFTs are presented. In essential, Ti ($4s^23d^2$) has a larger degree of orbital expansion than Si ($3s^23p^2$), a lower electronegativity (1.54) and a lower standard electrode potential (-1.63 V) compared to those of Zn (1.65 and -0.76 V). Most importantly, Ti-O (662 kJ/mol) has high BDE that can effectively reduce the defect density of the channel. [4] In addition to increase the crystallization temperature but also to decrease the degree of surface scattering caused by surface roughness, incorporation of Si in HfO_2 is expected to release interface matching problem by doping the same element Si with the channel layer.

Three types of TFTs based on HfO_2/SZTO (device A), $Hf_{1-x}Si_xO_2$/SZTO (devcie B), and $Hf_{1-x}Si_xO_2$/Ti-SZTO (device C) gate dielectric/channel structures are fabricated and comparisons of their electrical characteristics are made. Stability tests including hysteresis, positive (+4 V)/negative (-4 V) gate bias stress (GBS), white light exposure under reverse bias and heating tests are conducted. Results of device characteristics and threshold voltage shift (ΔV_{TH}) after stability tests are presented and discussed. Effects of the compositions of Ti and Si on TFT performances are clarified.

2. Experimental

Fig. 1 depicts the schematic cross section view of the SZTO and Ti-SZTO TFTs with a bottom HfO_2 or $Hf_{1-x}Si_xO_2$ gate dielectrics proposed in this study. The width/length of the channel layer is 200/20 μm. The fabrication process begins with the deposition of $Hf_{1-x}Si_xO_2$ gate dielectric layer with an equivalent oxide thickness (EOT) of 10±1 nm on n^+-type Si substrate. Various sputtering powers (0, 30, 40, and 50 W) were used for the Si target while that of the HfO_2 target was kept at 100 W. The ratio of Si/(Si+Hf) of the deposited dielectric layer is 0/12/18/25% based on XPS analysis. It was then followed by post-depositing annealing (PDA) at 600 ℃ for 10 min in O_2 ambient to improve layer quality.

For device fabrication, a 30-nm-thick Ti-SZTO channel layer was deposited by co-sputtering using SZTO (0.5 wt% Si, ZnO/SnO= 65/35) target and Ti target in Ar ambient at RT. The sputtering power for SZTO target was kept at 80 W and set Ti target power at 0, 30, 50 and 70 W, respectively. The Ti composition in the deposited films was 0/0.9/2.5/3.8 at% respectively, according to XPS analysis. After that, the samples were subjected to a PDA at 200 ℃ for 10 min in N_2 ambient. Subsequently, a patterned 25-nm-thick AZO buffer layer and a 150-nm-thick Ti metal were deposited as the source/drain electrodes. Finally, a 200-nm-thick SiO_2 passivation layer was deposited by sputtering to prevent devices deterioration (not shown).

To explore the effectiveness of Si doping in HfO_2 gate dielectrics on TFT performance, conventional SZTO TFTs with HfO_2 and $Hf_{0.82}Si_{0.18}O_2$ dielectric layers, called devices A and B (Figs. 1(a) and 1(b)) were fabricated. Note that $Hf_{0.82}Si_{0.18}O_2$ layer was chosen because it shows the best dielectric and interfacial characteristics among all test samples. Finally, TFTs with a co-sputtering deposited Ti (2.5%)-SZTO channel with $Hf_{0.82}Si_{0.18}O_2$ dielectric layers, called device C (Fig. 1(c)), was also prepared to clarify the effectiveness of Ti doping in channel.

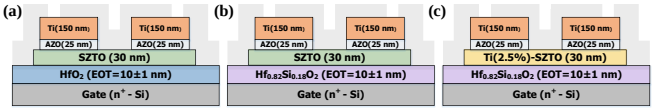

Fig. 1 Schematic cross section diagrams of the fabricated TFTs. (a) HfO_2/SZTO TFT (device A), (b) $Hf_{0.82}Si_{0.18}O_2$/SZTO TFT (device B), and (c) $Hf_{0.82}Si_{0.18}O_2$/Ti(2.5%)-SZTO (device C).

3. Results and Discussion

According to XPS analysis, C-V measurement, and AFM analysis, Si/(Si+Hf) ratio, κ value, and RMS of prepared $Hf_{1-x}Si_xO_2$ dielectric layer are summarized in Table I. It reveals that κ-value of the $Hf_{1-x}Si_xO_2$ dielectrics decreases with increasing Si content, attributing to the Si element was oxidized to form low-κ material SiO_2 after PDA in O_2 ambient. Moreover, $Hf_{1-x}Si_xO_2$ dielectrics have a higher transition temperature than that of HfO_2 as clarified by XRD analysis (Fig. 2(a)). It reveals that $Hf_{1-x}Si_xO_2$ still maintains the amorphous state after a thermal annealing at 600 ℃ and has the lowest RMS of 0.158 nm among all samples. Fig. 2(b) shows the J-V curve of MIM capacitors with HfO_2 or $Hf_{1-x}Si_xO_2$ dielectric film. All gate dielectrics are with EOT of 10±1 nm. The leakage current of the MIM structure of $Hf_{0.82}Si_{0.18}O_2$ is nearly 2 orders lower than HfO_2, which is the best performance among all samples.

Figs. 3(a) and 3(b) show the O 1s core-levels XPS spectra of the annealed Ti-SZTO films. It indicates that the content of Ti is 0/0.9/2.5/3.8 at% in Ti-SZTO films deposited by sputtering power of 0/30/50/70 W, and the ratio of V_O (O_{II}/O_T) is about 30.3/21.8/18.6/23.9%, respectively.

These results confirm that Ti incorporation in SZTO film could serve as a good V_O inhibitor to reduce internal defects in the film. Fig. 3(c) depicts the transfer characteristics of devices A, B and C. A comparison of electrical parameters of devices are listed in Table II, which also compares some other data reported in the literature. The results shows that device B exhibits better electrical properties than device A with an on/off current ratio (I_{on}/I_{off}) of 9.79×10^7, threshold voltage (V_{TH}) of 0.32 V, subthreshold swing (SS) of 98 mV/dec, field effect mobility (μ_{FE}) of 31.6 $cm^2\cdot V^{-1}\cdot s^{-1}$, and interface trapped density (D_{it}) of 1.23×10^{12} $cm^{-2}\cdot eV^{-1}$. The reduction of I_{off} is evident, it indicates that the appropriate doping of Si in HfO_2 could reduce V_O and surface roughness to suppress trap density at the dielectrics/channel interface. In addition, device C shows the best gate controllability and I_{on} with an I_{on}/I_{off} of 2.78×10^8, V_{TH} of 0.23 V, SS of 87 mV/dec, μ_{FE} of 36.8 $cm^2\cdot V^{-1}\cdot s^{-1}$, and D_{it} of 8.97×10^{11} $cm^{-2}\cdot eV^{-1}$. Note that the suppression in D_{it} is responsible for the improved SS and μ_{FE} of TFTs. It attributed to suitable incorporate Ti in SZTO channel might not only reduce the density of bulk defects but also improve the quality of interface with dielectric.

Table I Si/(Si+Hf) ratio, dielectric constant and roughness of $Hf_xSi_{1-x}O_2$ films prepared by different co-sputtering power combinations.

Power ratio: HfO_2/Si (W)	Si/(Si+Hf) (%)	Dielectric	κ	Roughness (nm)
100/0	0	HfO_2	27.8	0.848
100/30	12	$Hf_{0.88}Si_{0.12}O_2$	22.6	0.202
100/40	18	$Hf_{0.82}Si_{0.18}O_2$	21.4	0.158
100/50	25	$Hf_{0.75}Si_{0.25}O_2$	20.5	0.169

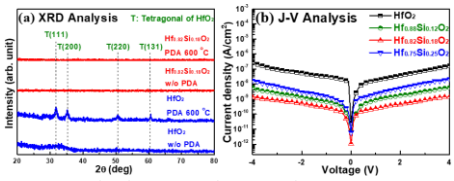

Fig. 2 XRD analysis of HfO_2 and $Hf_{1-x}Si_xO_2$ films without and with PDA at 600 ℃ for 10 min in O_2 ambient. (b) J-V curve of MIM capacitors with HfO_2 and $Hf_{1-x}Si_xO_2$ dielectrics after PDA at 600 ℃ for 10 min in O_2 ambient.

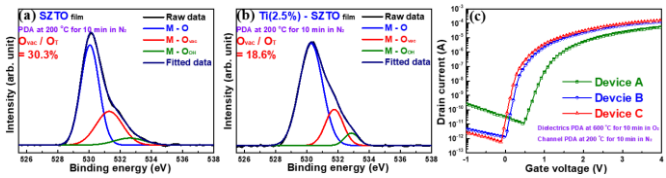

Fig. 3 O 1s core-levels XPS spectra of (a) SZTO and (b) Ti(2.5%)-SZTO (c) transfer characteristics of devices A, B, and C.

Table II Electrical parameters of devices prepared in this study

Device	I_{on}/I_{off}	V_{TH} (V)	SS (mV/dec)	μ_{FE} ($cm^2/V\cdot s$)	D_{it} ($cm^{-2}eV^{-1}$)
A	5.28×10^6	0.89	162	17.1	3.69×10^{12}
B	9.79×10^7	0.32	98	31.6	1.23×10^{12}
C	2.78×10^8	0.23	87	36.8	8.97×10^{11}
[5]	6.1×10^7	-2.8	1110	49.88	-
[6]	8.03×10^8	2.39	430	13.33	-

Fig. 4 illustrates the hysteresis loops of devices A, B, and C under forward (-1 V to 4 V) and reverse (4 V to -1 V) sweeps. The transfer curves of the three devices are all shift to the right, indicating that the polarity of the trapped charges is negative. Note that device B has a lower $\Delta V_{TH(Hys)}$ of 0.085 V as compared to 0.31 V of device A, suggesting the effectiveness of Si incorporation in HfO_2. Furthermore, a much less $\Delta V_{TH(Hys)}$ of 0.018 V shown by device C indicates the incorporation of Ti in SZTO channel being effective to reduce excessive V_O therein.

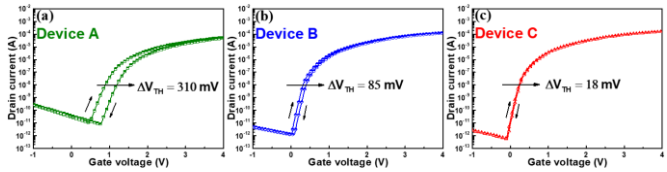

Fig. 4 Hysteresis loops of (a) device A, (b) device B, and (c) device C under the forward (-1 to 4 V) and revers (4 to -1 V) sweeps.

Fig. 5 shows the transfer characteristics of device C after +4 V (PGBS), -4 V (NGBS), and white light illumination (0.5 mW/cm^2) at -2 V for 0, 10, 100, and 1000 s, as well as thermal test from 298 to 378 K for 1000s, respectively. The threshold voltage shift (ΔV_{TH}) as a function of stress time for devices A, B and C is also shown in the inset of the figure. The values of ΔV_{TH} after 1000 s reliability tests are listed in Table III, which also compares some other data reported in the literature. It is noted that device C has the best reliability test results. As compared to device A, device shows about 83% and 84% reduction in ΔV_{TH} after PGBS and NGBS for 1000 s. It confirms that the incorporation of Si in HfO_2 dielectrics and Ti in SZTO channel layer could reduce the amount of trapping charges to promote device stability.

White light illumination provides electronic energy for electrons in deep and shallow state defects of V_O to migrate to E_C. The increments of free electrons in the channel then causes the reduction of gate control and negative shift of ΔV_{TH}. After light illumination under -2 V for 1000 s, it is found that the ΔV_{TH} of device B decreases from -0.569 V to -0.306 V (~ 45% reduction) as compared with device A. It is mainly attributed to the $Hf_{0.82}Si_{0.18}O_2$/SZTO system which has large valence band offset to resist a photo-created holes injection to gate dielectric. Note that device C has a further decreased ΔV_{TH} (from -0.306 V to -0.165 V, ~ 46% reduction) as compared with that of device B. indicating that the SZTO channel with Ti incorporation could effective reduce defects and exhibit excellent light stability. Finally, after heating test, device C shows a significant improvement from -0.419 V to -0.105 V (~ 75% reduction) as compared with device A. Our experimental results shown above confirm that the effectiveness of incorporation of Si in HfO_2 dielectric layer and Ti in SZTO channel layer is effective in reducing excessive defects, which could improve interface quality to promote device performances and reliability.

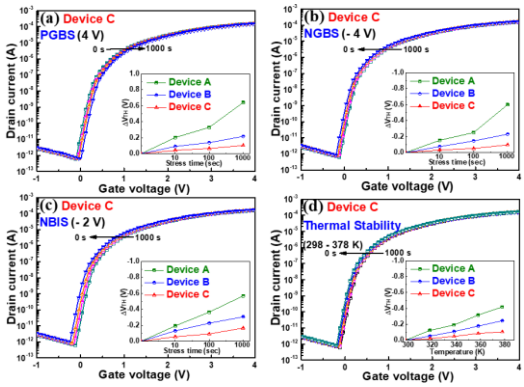

Fig. 5 The transfer characteristics of device C under (a) PGBS, (b) NGBS, (c) NBIS, and (d) thermal stability tests. The inset in these figure shows the measured ΔV_{TH} as a function of stress time for devices A, B, and C.

Table III ΔV_{th} after each stability tests for 1000 s

ΔV_{th} (V) (1000 s)	PGBS	NGBS	NBIS	TS (378 K)
A	**0.642**	**- 0.601**	**- 0.569**	**- 0.419**
B	**0.217**	**- 0.231**	**- 0.306**	**- 0.245**
C	**0.103**	**- 0.096**	**- 0.165**	**- 0.105**
[5]		- 0.75		
[6]				- 0.91

4. Conclusions

Ti (2.5%)-SZTO TFTs with $Hf_{0.82}Si_{0.18}O_2$ gate dielectrics with much improved electrical performance and stability have been demonstrated. As compared with conventional HfO_2/SZTO TFT(device A), the proposed $Hf_{0.82}Si_{0.18}O_2$/Ti(2.5%)-SZTO TFT (device C) show a significant suppression in ΔV_{TH} with 94%, 83%, 84%, 71%, and 75% after hysteresis and PGBS, NGBS, NBIS, TS (at 378 K) tests for 1000 s, respectively. It is expected that the $Hf_{0.82}Si_{0.18}O_2$/Ti(2.5%)-SZTO TFTs proposed and demonstrate in this study could be very potential for applications in advanced displays and flexible electronics.

Acknowledgements

This work was supported by the Ministry of Science and Technology (MOST), Taiwan, under contract MOST 108-2221-E-006-039.

References

[1] S. Aikawa *et al.*, Jpn. J. Appl. Phys. **58** (2019) 090506.
[2] C. Wu *et al.*, Appl. Phys. Lett. **103** (2013) 082109.
[3] L. P. Feng *et al.*, Vacuum **83** (2009) 902.
[4] H. H. Hsu *et al.*, IEEE Electron Device Lett. **35** (2014) 87.
[5] B. H. Lee *et al.*, Physica B Condens. Matter **574** (2019) 311.
[6] J. Y. Hwang *et al.*, Solid State Electron. **153** (2019) 93.