Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp709-710

Effects of Post Deposition Annealing on the Solid-Phase Crystallization of Ge Leading to a Hole Mobility of 530 cm^2 V^{-1} s^{-1} on Glass

Takuto Mizoguchi[1], Toshifumi Imajo[1], Takashi Suemasu[1], and Kaoru Toko[1]

[1] Institute of Applied Physics, University of Tsukuba, 1-1-1 Tennodai, Tsukuba, Ibaraki 305-8573, Japan
Phone: +81-29-853-5472, E-mail: mizoguchi.takuto.sj@alumni.tsukuba.ac.jp

Abstract

The solid-phase crystallized Ge thin film on a glass substrate exhibited a hole mobility exceeding 530 cm^2 V^{-1} s^{-1} without thickening Ge or preparing an underlayer. The key technology was the post deposition annealing for amorphous Ge precursors, which improves the crystallinity of the resulting polycrystalline Ge.

1. Introduction

Ge on insulator technology has been widely studied for lowering the fabrication cost and improving the device performance of thin film transistors. Solid-phase crystallization (SPC) is a simple method to directly form polycrystalline Ge (poly-Ge) thin films on glass substrates at low temperatures. Recently, we found that the condition of the amorphous Ge (a-Ge) precursors strongly affects the subsequent SPC [1]. Here we investigate the effects of the post deposition annealing (PDA) of a-Ge precursors on the resulting SPC-Ge.

2. Experimental Procedure

Figure 1(a) shows the schematic of sample preparation. The a-Ge precursors (150 nm thick) were deposited on SiO_2 glass substrates using the Knudsen cell of a molecular beam deposition system (base pressure: 5×10^{-7} Pa) while heating the samples at 125 °C. After that, PDA was performed for 2 h in the same vacuum chamber. The PDA temperature, T_{PDA}, was ranged from 300 to 700 °C. For comparison, the sample without PDA (T_{PDA} = RT) was also prepared. Then, the samples were loaded into a conventional tube furnace in a N_2 atmosphere and annealed to induce SPC. The growth temperature, T_{SPC}, was 450 °C for 5 h or 375 °C for 150 h. Subsequently, we performed post annealing (PA) at 500 °C for 5 h in an Ar atmosphere. The samples were evaluated using Raman spectroscopy, electron backscattering diffraction (EBSD) analysis, and Hall effect measurements.

3. Results and Discussion

The Raman spectra in Fig. 1(b) shows sharp peaks near 300 cm^{-1} corresponding to crystalline Ge only for T_{PDA} = 700 °C, while no peaks are observed for T_{PDA} < 700 °C. Figure 1(c) shows that all samples for T_{SPC} = 450 °C exhibit sharp peaks corresponding to crystal Ge. These results indicate that the Ge nuclei start to form in the a-Ge layer above 700 °C in vacuum, while below 450 °C in N_2 after air exposure. Raman shift and the full width at half maximum (FWHM) of the Ge-Ge peaks are summarized in Fig. 1(d). All peaks shift to lower wavenumbers than that of a bulk Ge substrate, originating from the tensile strain due to the difference of the thermal expansion coefficient between Ge and the SiO_2 substrate [1]. The peak shift increases with increasing T_{PDA} and turns to de

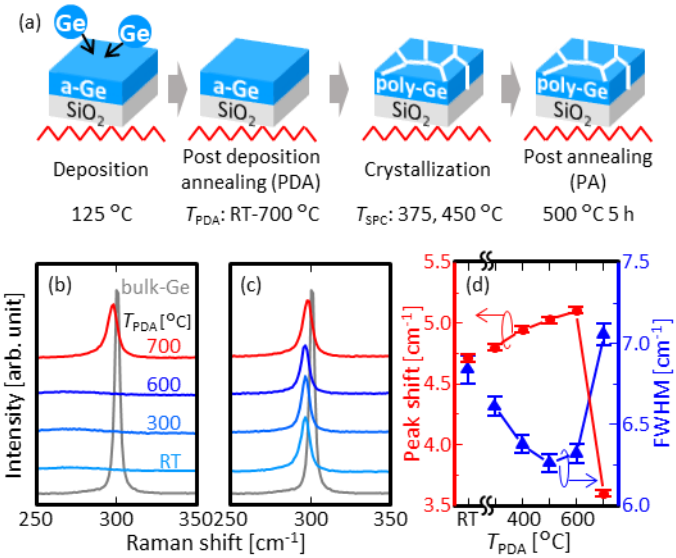

Fig. 1 (a) Schematic of sample preparation. Raman spectra (b) after PDA and (c) after SPC (T_{SPC} = 450 °C) of samples with various T_{PDA}. (d) T_{PDA} dependence of Raman shift and FWHM.

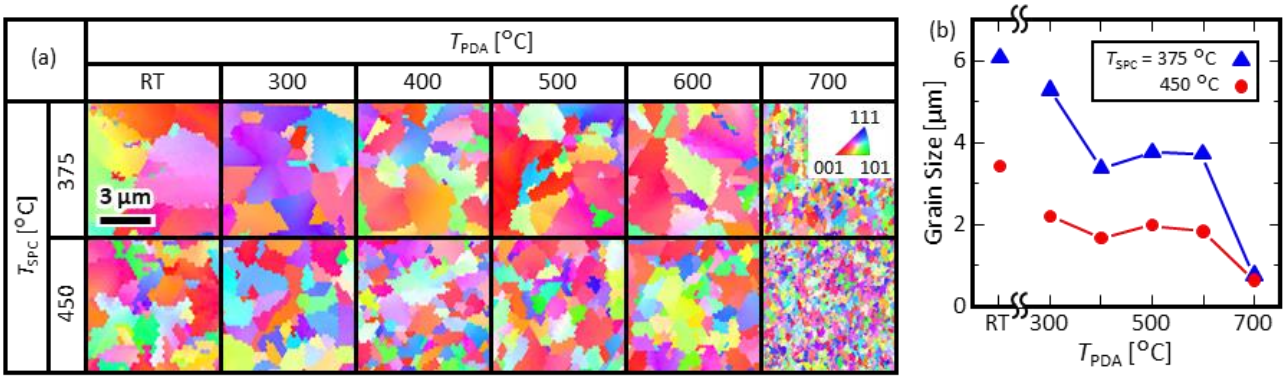

Fig. 2 (a) EBSD images after SPC (T_{SPC} = 375, 450 °C) of samples with various T_{PDA}. (b) T_{PDA} dependence of grain size.

crease at 700 °C. Conversely, FWHM decreases with increasing T_{PDA} and turns to increase at 600 °C. These behaviors are explained later in terms of grain size.

The EBSD images in Fig. 2(a) show that the grain size depends on both T_{PDA} and T_{SPC}. Figure 2(b) shows that the samples with PDA have smaller grains than the samples without PDA (T_{PDA} = RT), which indicates that PDA promotes nucleation rather than lateral growth. For T_{PDA} < 700 °C, the lower T_{SPC} provides a larger grain size, which agrees with the basic behavior of SPC [2]. On the contrary, the T_{PDA} = 700 °C sample has quite small grains regardless of T_{SPC}, which is likely due to the crystallization during the PDA. This result accounts for the high FWHM due to the low crystallinity and the low peak shift due to the strain relaxation at grain boundaries (Fig. 1). Conversely, the T_{PDA} = 500 °C sample showed the lowest FWHM value (Fig. 1(d)) despite its small grain size, which suggests that the T_{PDA} = 500 °C sample has relatively few intragranular defects.

In Hall effect measurements, all samples showed p-type conduction, similar to conventional undoped SPC-Ge [1,2]. As shown in Fig. 3(a), for both before and after PA, hole concentration p increases with T_{PDA}. Considering the T_{PDA} dependence of the grain size, this behavior is due to the increase of acceptors from the grain boundaries. Figure 3(b) shows that, for each T_{PDA}, the lower T_{SPC} provides the higher hole mobility μ due to the larger grain size, that is, the weaker grain boundary scattering. After PA, μ improves for all the samples due to the decrease of the impurity scattering. The T_{PDA} = 500 °C sample exhibits the peak μ value reaching 530 cm^2 V^{-1} s^{-1}.

To explain this behavior, we investigated the energy barrier height (E_B) of the grain boundary from temperature (T) dependence of μ. Figure 3(c) suggests that μ is limited by both impurity scattering and grain boundary scattering near RT while only by grain boundary scattering at low temperature [3]. Figure 3(d) shows that PDA reduces E_B, whereas the trap state density (Q_t) is almost the same. After PA, the E_B difference due to PDA becomes more pronounced. This behavior results from E_B reflecting p and Q_t, where PA lowers both p and Q_t. Therefore, the high μ of the T_{PDA} = 500 °C sample is considered to originate from the proper balance between p and Q_t.

As shown in Fig. 4, the Ge layer proposed in this study exhibits high μ (530 cm^2 V^{-1} s^{-1}) among Ge on insulators. The μ value is higher than any other Ge layers directly synthesized on a glass substrate without underlayer and those with the film thickness below 200 nm. Therefore, PDA is effective in modulating the crystallinity and electrical properties of Ge layers, which should be controlled according to the other conditions.

4. Conclusions

We investigated the effects of the PDA process on the SPC-Ge. PDA at appropriate temperature (500 °C) reduced grain size while improving crystallinity, which led to the reduction of E_B. The resulting hole mobility (530 cm^2 V^{-1} s^{-1}) is the highest value among that of Ge layers on glass synthesized at low temperatures without underlayer. The finding will improve the TFT performance based on Ge thin films.

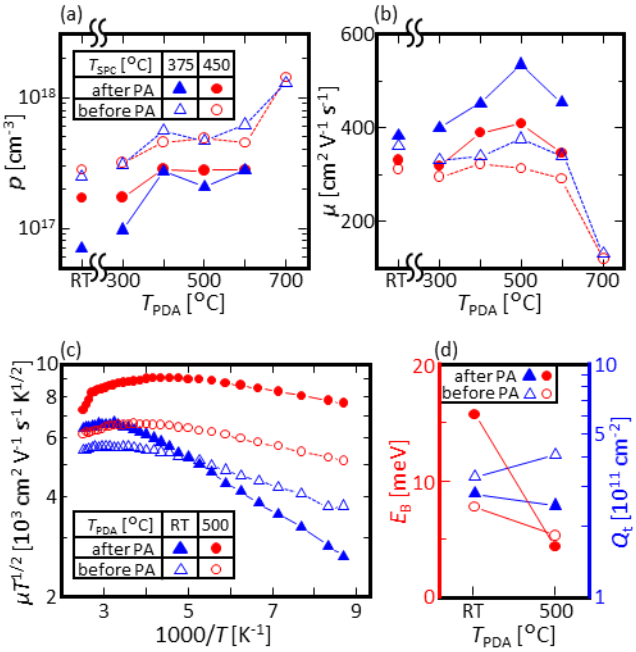

Fig. 3 T_{PDA} dependence of (a) hole concentration and (b) hole mobility before and after PA with T_{SPC} = 375 and 475 °C. (c) Arrhenius plot of $\mu T^{1/2}$, (d) Energy barrier E_B and trap-state density Q_t for grain boundaries of samples with T_{PDA} = RT and 500 °C. Here, T_{SPC} = 375 °C.

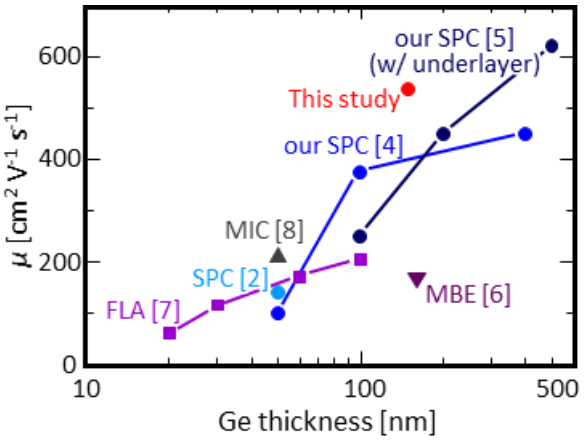

Fig. 4 Comparison of hole mobility and thickness of Ge films on insulators.

References

[1] K. Toko *et al*., Sci. Rep. **7**, 16981 (2017).
[2] K.Toko. *et al*., Solid-State Electron. **53**, 1159 (2009).
[3] J. W. Seto, J. Appl. Phys. **46**, 5247 (1975).
[4] R. Yoshimine. *et al*., Appl. Phys. Express. **11**, 031302 (2018).
[5] T. Imajo *et al*., Appl. Phys. Express. **12**, 015508 (2019).
[6] O. Nakatsuka *et al*., Jpn. J. Appl. Phys. **49**, 04DA10 (2010).
[7] K. Usuda *et al*., Appl. Phys. Express **7**, 56501 (2014).
[8] K. Kasahara *et al*., Appl. Phys. Lett. **107**, 142102 (2015).