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Fully Integrated Hybrid Digital LDO / Switched Capacitor Voltage Regulator for Power Delivery of SOC Standby Power Rail

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Abstract

A fully integrated hybrid digital LDO / switched capacitor (SC) voltage regulator (VR) was developed. Proposed VR automatically detects the load current to determine the mode of its operations, LDO or SC VR mode. It deploys a proportional-differential-and-averaging comparator for pole / zero control. Silicon measurement shows that, in SC VR mode, the power conversion efficiency is 30 % better than that of the ideal LDO, while it delivers equivalent efficiency to LDO when load current is above SC VR capability.

1. Introduction

The switched capacitor (SC) voltage regulator (VR) [1-4] is the DC-DC converter that has an advantage in delivering a light load current, but it is not widely used as a fully integrated solution of SOC due to the cost of on-die capacitors in product context: The highest load current that SC VR can deliver is limited by the amount of fly capacitors. This paper presents the hybrid digital LDO / SC VR that was developed for the real product on 14nm process node, which delivers power to the stand-by power supply rail. The capability of digital LDO was added due to the following reason: During standby state of SOC, the nominal load current is very limited (up to 30~40 mA), but the peak current can be as high as 300 mA, though it does not happen very often. If traditional SC VR needs to support this high current, the fly capacitor needs to be significantly increased, which is not realistic in the product context. A hybrid digital LDO / SC VR is the solution.

2. Circuit Implementation

The proposed hybrid VR receives the input voltage (VIN = 1.8V), and it down-converts to the lower output voltage (VOUT). The functional block diagram of the proposed VR is depicted in Fig. 1. The voltage regulation of the proposed VR is based on the switch resistance modulation [1] to control the output voltage (VOUT) for different load currents. In SC VR mode, two different divider ratios are supported: 2/3 and 1/2. The operational frequency of the digital control is 60 MHz, but it is the 4-way interleaved structure to reduce the output voltage ripple. It deploys the switched capacitor (SC) proportional-differential-and-averaging (PDA) comparator. The traditional PID digital control requires ADC to capture the feedback voltage, but most of SC VRs reported in academics simply use a comparator rather than ADC [1-4] due to simplicity of the design. However, the comparator-based solution has a concern on the loop stability due to a lack of control on poles and zeros. Proposed SC PDA comparator addresses this issue. The operation of SC PDA comparator is based on the following:

$$X = \omega_1(V_{FEEDBACK} - V_{REF}) + \omega_2 \frac{dV_{OUT}}{dt} + \omega_3 E_{T=RC}[V_{FEEDBACK} - V_{REF}] \quad (1)$$

where $E_{TC=RC}[X]$ indicates the average on X during the period $T=RC$. X in Eqn. (1) is the weighted sum of the proportional, differential, and averaging terms, from which the comparator makes a decision. The differential branch of SC PDA comparator injects a zero to the feedback loop and improve the phase margin. The averaging branch of SC PDA comparator adds a pole and reduces the impact of the aliasing noise, which is a common issue for the digital feedback control. Fig. 2 shows the circuit implementation of SC PDA comparator. It is a simple extension of the conventional inverter based switched capacitor comparator [5], to which, the differential and averaging branches are added. Embedded auto-zeroing enables mV level of accuracy without calibration. Fig. 3 shows the finite state diagram of the digital feedback controller. It is the up / down counter-based control as the traditional digital LDO, and additionally, there is a capability to keep track of whether VR is in LDO or SC VR mode. Higher state number in Fig. 3 indicates the higher load current state, and up / down control is based on the comparator output value. Transition between SC VR and LDO modes creates a discontinuity, which can be a risk for seamless transition between two modes. In order to avoid the corner case limit cycling scenario at the boundary of two modes, the transition from LDO back to SC VR is prohibited for the next 10 cycles, once VR gets into LDO mode. Fig. 4 depicts the topology of power MOS switches. The upper left view is the one with 2/3 divider ratio and the upper right view is the one with 1/2 divider ratio in SC VR mode. In SC VR mode, the switch resistance is controlled by turning on and off transistor banks. The lower left view is the power MOS usage in LDO mode, where the switch resistance is controlled based on the programmable bias current.

3. Measurement Result

Fig. 5 shows the measured power conversion efficiency of the proposed VR across different load currents. The upper graph is for VOUT=1.02 V and 2/3 SC VR divider ratio, while the lower graph is for VOUT=0.79 V and 1/2 SC VR divider ratio. When VOUT = 1.02 V, the proposed VR outperforms the ideal LDO by 20 % in peak and when VOUT = 0.79 V, the proposed VR outperforms the ideal LDO by 30 % in peak. Above 100 mA of the load current, the efficiency of the proposed VR is almost equivalent to that of the ideal LDO. Upper graph in Fig. 6 shows the measured time domain waveform of VOUT with differentiation on and off when the load current is 250 mA. The waveform proves the effectiveness of the differentiation capability of SC PDA

comparator. In order to evaluate the seamless transition between SC VR and LDO modes, the efficiency and the output voltage ripple of VR are captured from one of the silicon units, with every 2 mA of the load current around the transition between SC VR and LDO modes, which is shown as the lower graph in Fig. 6. The voltage ripple vs. load current curve is smooth without glitches during the transition between SC VR and LDO modes, which indicates that the seamless transition is achieved.

References

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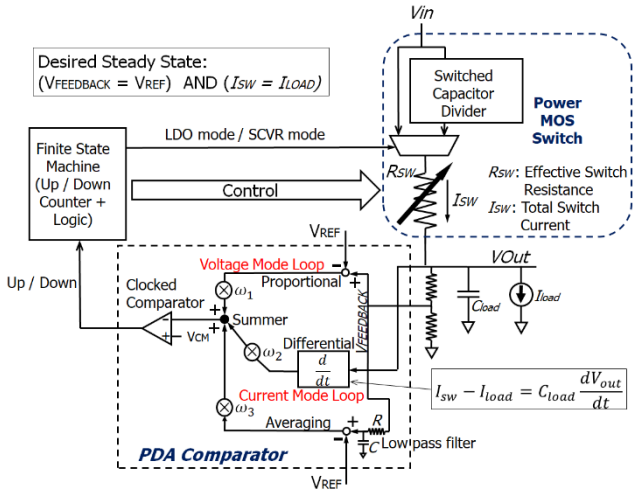

Fig. 1: Functional Block Diagram of Proposed Hybrid Digital LDO / Switched Capacitor Voltage Regulator

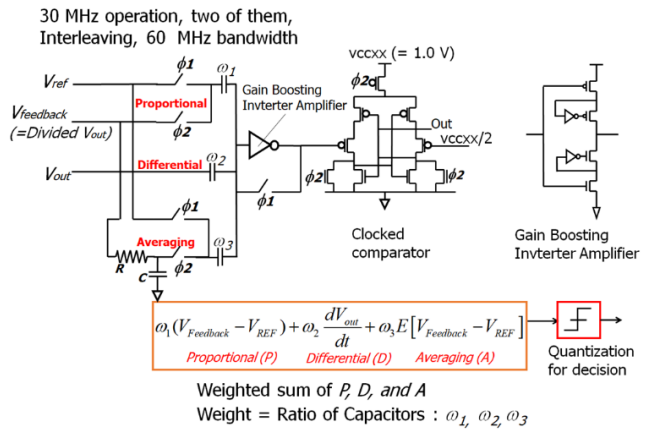

Fig. 2: Proposed Switched Capacitor (SC) Proportional–Differential-and-Averaging (PDA) Comparator Circuit Implementation

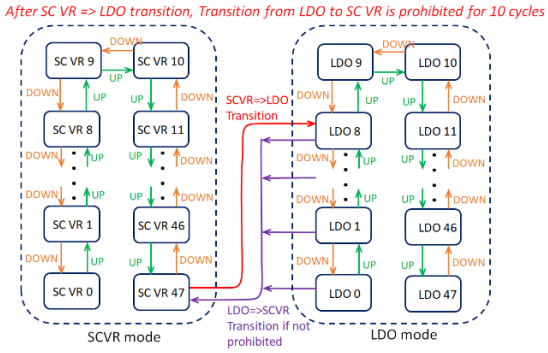

Fig. 3: Finite State Diagram of Proposed Hybrid Digital LDO / SC VR Digital Feedback Controller

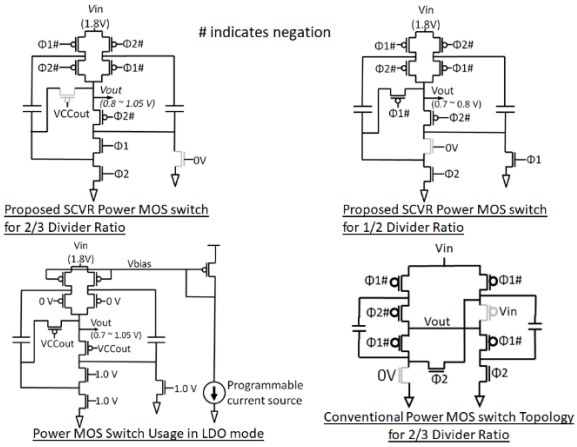

Fig. 4: Power MOS Switch Topology (Proposed vs. Conventional)

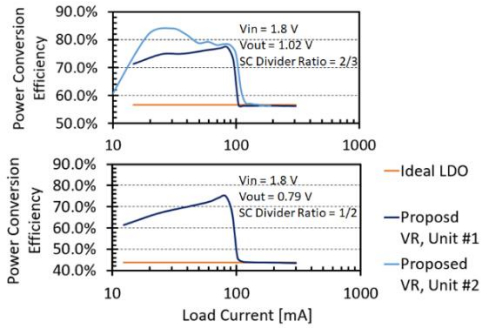

Fig. 5: Power Conversion Efficiency of Proposed Hybrid Digital LDO / SCVR Regulator (Measured)

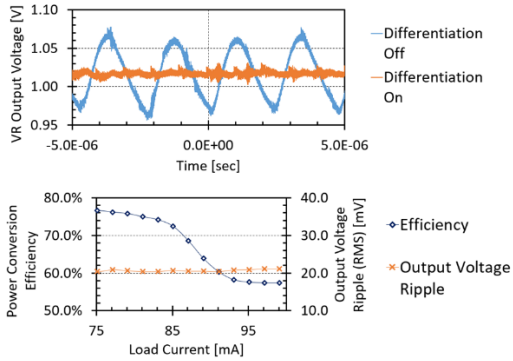

Fig. 6: Upper: Time Domain Waveform of VR Output Voltage with Comparator Differentiation Term On / Off, under Load Current = 250 mA (Measured), Lower: Evaluation of Seamless Transition between LDO and SCVR Modes (Measured)