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A 0.7µm CMOS Image Sensor with 24,000e- FWC Using 1:4 Dual Conversion Gain Technology for High SNR Performance

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Abstract

This paper introduces the world's first 0.7µm pixel CMOS Image Sensor (CIS) with 1:4 Dual Conversion Gain (DCG) pixel technology. The new scheme, FD-Shared structure is designed to apply the 1: 4 DCG technology. This technology has made it possible to achieve FWC 24,000e- at 0.7µm pixel and it can have the better optical characteristics as 1.4µm pixel in four FD sum mode. We have confirmed that it had the same dark noise performance as previous work [1], and Signal-Noise Ratio (SNR) performance at high lux condition is improved by 6dB compared with Single CG. DCG technology is one of the effective ways to improve FWC and will be useful as the pixel size becomes smaller.

1. Introduction

In recent years, the high-resolution demand for the CMOS image sensor market for mobile has continuously increased [2], so the pixel size has been decreased to 0.7µm. The optical performance at low light condition has been decreased due to reduction of pixel pitch, however the tetra cell technology helped solve this problem. The tetra cell technology was able to achieve performance of large pixels by merging four pixels. For example, if high resolution is required, resolution of 0.7µm pixel can be used. If high sensitivity is required, four pixels are merged using tetra cell technology and used as 1.4µm pixel. In order to fully use the electrons generated in four photodiodes when merging four pixels, Conversion Gain (CG) needs to be lowered to 1/4, which requires 1:4 Dual Conversion Gain (DCG) technology. The 1:4 DCG pixel technology of the floating diffusion (FD)-shared structure is more advanced technology and improve the FWC performance of the tetra cell up to 24,000e-. This technology doubles the full well capacity (FWC) performance compared to the conventional 1:2 DCG pixel technology which was used in 0.8µm pixel [3], and it maximize the advantages of tetra cell.

2. Technology

DCG technology with FD-Shared type

CG is one of the factors that determine output sensitivity and available FWC. The unit of CG is defined as µV/e- and the output sensitivity increases and the available FWC decreases as CG increase. For this reason, if CG can be changed with the same sensor, it would be used efficiently in light and dark situations. In order to maximize the advantages of CG values, "Dual" CG technology using both high and low CG at the same time has been developed.

Dual CG technology generally consists of circuits that control FD capacitance. In addition, the ratio of DCG is determined according to the size of the FD capacitance and the additional one. As the Pixel size becomes smaller, the physical space to create additional capacitance for DCG is reduced. In order to overcome the problem of physical space, this paper presents an FD-shared type DCG technology that obtains additional caps using the FD of $n+1_{th}$ row. This can solve the spatial limitations of the additional capacitance for 1:4 DCG technology. Figure 1 shows the conventional DCG method and the DCG type of the method proposed in this work.

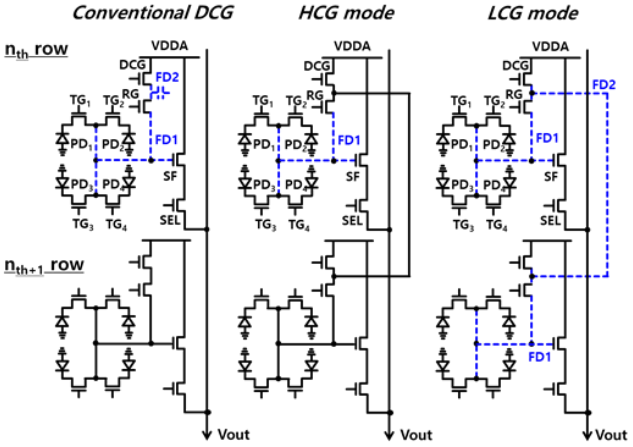

Fig. 1 DCG Structures, Conventional and FD-Shared

DCG Operation

The spatial limitations of DCG technology are solved through the FD-shared structure as described in the previous subsection. A new timing scheme is needed to implement the 1: 4 DCG scheme. A simple timing diagram is shown in Figure 2 and each timing is described as follows.

In high conversion gain (HCG) mode, the reset gate (RG) transistor is "always on" and the DCG transistor is responsible for the reset operation. The HCG mode operates using only the n_{th} row, such as conventional single CG operation.

In low conversion gain (LCG) mode, RG and selection (SEL) transistor must operate at the same time in n_{th} and $n+1_{th}$ row. At this time, the DCG transistor is "always on"

and the RG transistor is in charge of the reset operation.

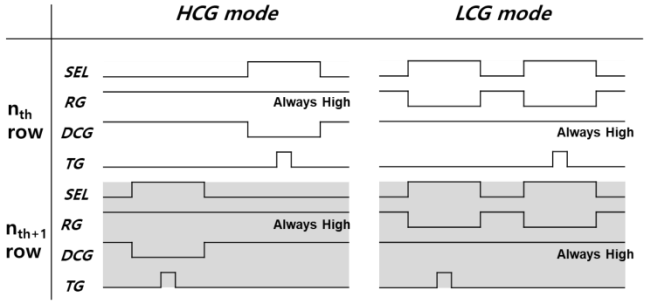

Fig. 2 DCG Operation, HCG mode and LCG mode

Fabrication

FWC inevitably becomes smaller as the pixel size becomes smaller and the FWC trend as a function of pixel pitch shown in figure 3. In order to minimize the decrease in FWC, the physical volume of the photodiode must be maximized. In this work, FWC of 6,000e- was achieved even in 0.7μm pixel using full depth-DTI technology which has advantages in FWC in small pixel [4]. With these approaches, we were able to achieve the same level of FWC as the previous generation [3,5].

Characteristics

As the pixel has shrink, pixel merging method has been adapted to provide a large-pixel's performance. Even if pixel merging using tetra cell technology, FWC cannot be increased due to the Analog Digital Converter (ADC) saturation range and FD dynamic range limitation. However, with the 1:4 DCG scheme, it enables to increase FWC in a fixed ADC saturation range.

Figure 3 shows the photon transfer curve of the HCG and LCG respectively, and the LCG decreases by 25% in its value compared to the HCG, and with the 1/4 CG, it can quadruple the FD dynamic range resulting in 4 times of FWC than HCG's. All electrons from the four photodiodes can be represented when dynamic range of the FD is quadrupled in the structure that shares four FDs. For this reason, 1:4 DCG is a perfect combination with four FD shared structure.

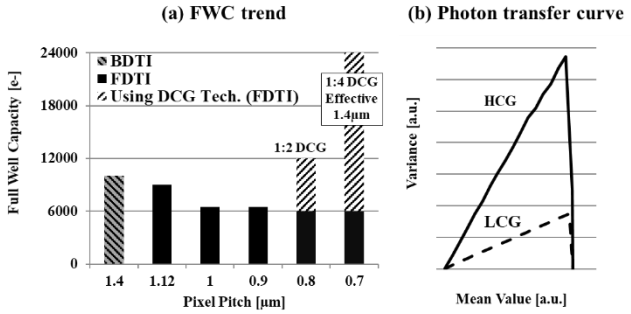

Fig. 3 (a) FWC trend according to pixel pitch and (b) Photon Transfer Curve of 1:4 DCG Pixel

FWC and SNR performances are summarized in Table I. FWC is improved by applying the 1:4 DCG technology and SNR at high illuminance condition is also increased as a result of high FWC. FWC increases from 6,000 to 24000e- in the full and binning mode, respectively. High and 20 lux SNR is improved by 6dB and 6dB, respectively. it is improved by 6dB and dark noise performance is the same as previous work [1].

By using tetra cell technology with 0.7μm, an effective pixel pitch is equivalent to 1.4μm and the FWC of 1.4μm pixel is about to ~10,000e-. The FWC of the 0.7μm merged pixel with 1: 4 DCG technology is superior to that of the 1.4μm pixel in terms of SNR at high illumination condition since FWC of merged 0.7μm pixel is higher than that of 1.4μm pixel.

Table I 1:4 DCG Characteristics

Characteristics	Unit	0.8μm Single CG [3,5]	0.7μm Single CG [1]	0.7μm Dual CG (1:4)	
Linear full-well capacity	e-	6,000	6,000	6,000	24,000
High Lux SNR	dB	44.0	43.0	43.0	49.0
20 Lux SNR	dB	26.0	25.0	25.0	31.0
RN	e-	1.4	1.4	1.2	4.5
RTS	ppm	3	3	4.5	0.1
WS	ppm	20	20	20	16

3. Conclusions

1:4 DCG pixel with 0.7μm is introduced and we have developed the FD-shared type structure in order to solves space limitations. A new timing scheme is also introduced to operate FD-shared type DCG pixel. The effective pixel pitch of 0.7μm pixel using tetra cell technology is 1.4μm, and it is possible to achieve 24,000e- of FWC, which is more than twice that of the previous 1.4μm pixel. Out pixel shows higher SNR than 0.7μm Single CG pixel and it is improved by 6dB. The development of this technology makes it possible to reduce the pixel size further and maximize the number of pixels.

References

[1] H. Kim et al, "A 1/2.65in 44Mpixel CMOS Image Sensor with 0.7μm Pixels Fabricated in Advanced Full-Depth Deep-Trench Isolation Technology", ISSCC, Feb. 2020.

[2] A. Suzuki et al., "6.1 A 1/1.7-inch 20Mpixel Back-illuminated stacked CMOS image sensor for new imaging applications," ISSCC, pp. 1-3. Feb. 2015.

[3] D. Jang et al, "0.8㎛-pitch CMOS Image Sensor with Dual Conversion Gain Pixel for Mobile Applications", IISW, June 2019.

[4] Y. Kim et al, "A 1/2.8-inch 24Mpixel CMOS image sensor with 0.9μm unit pixels separated by full-depth deep-trench isolation", ISSCC, Feb. 2018.

[5] D. Park et al, "A 0.8 μm Smart Dual Conversion Gain Pixel for 64 Megapixels CMOS Image Sensor with 12k e-Full-Well Capacitance and Low Dark Noise", IEDM, Dec. 2019.