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One Chip Mixer-Based Subarray Beamformer for Ultrasound Imaging with Sub-Nyquist Rate ADC

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Abstract

In this study, we propose a one chip mixer-based subarray beamformer for ultrasound imaging, fabricated using a 65-nm CMOS process. In the proposed beamformer circuit, signal processing is performed in I and Q-phases, in which each path can be obtained using only one operational transconductance amplifier. The fabricated chip achieves mixing, addition, and filtering operations for 8 input signals with a 0.4 mW/Ch power dissipation.

1. Introduction

Ultrasound imaging has become an important and useful technique for point-of-care medical diagnosis compared with other imaging techniques [1]. Generally, ultrasound imaging uses several transducer elements for tissue visualization with the spatial resolution dictated by the array aperture. High-resolution arrays require large transducer counts, resulting in high data rates and digital processing complexity in the backend. As transducer counts and portability becomes more important, reducing the power consumed by the imager becomes critical. To meet the above requirements, compressed-sensing (CS) techniques for ultrasound imaging have been much attracted and some studies are presented. For example, an entire framework was proposed in [2], enabling compressed ultrasound imaging using the mixer-based subarray beamformer, and it revealed that the framework can reduce up to 1/28 compared with standard beamforming sampling rate without substantial image quality degradation. Moreover, an advantage of employing the mixer-based subarray beamformer was reported from PCB-based hardware implementation of an analog front-end [3]. However, there have never been any reports regarding the development of one chip mixer-based subarray beamformer.

This paper builds on the previously cited work [3] by introducing a single-chip solution which implements the mixer-based subarray beamforming operation, capitalizing on silicon integration to achieve further reduction in power and area. Initially, the specifications required for the beamformer in the ultrasound imaging system were clarified. Thereafter, we derived a new topology of a mixer-based subarray beamformer circuit. Finally, we designed a one chip mixer-based subarray beamformer through a 65-nm CMOS process.

2. Design of System and Beamformer Circuit

The proposed subarray beamformer, which has 8 input signal ports, consists of a mixer, an adder, and a filter to achieve mixer-based beamforming. Initially, specifications of the beamformer such as the required dynamic range (DR) and bandwidth (BW) were determined by simulation in a MATLAB environment. The signal chains with various BW and DR were prepared, and the image qualities were checked. Considering the results, BW and DR of entire signal chain were set to 1.25MHz and 65dB, respectively. Simulation result using 64 channels with the above BW and DR is Fig.1 (b). The sampling rate of the ADC in the designed system is 1/8 of the sampling rate used to obtain the reference image (Fig.1(a)). Comparing with Fig. 1(a), the image quality deterioration of Fig.1(b) is suppressed, although sampling rate can be reduced thanks to CS technique. From the above information, DR of the beamformer part was assigned to 72dB.

Fig. 2 illustrates our designed mixer-based 8 input signal subarray beamformer. The important feature of this circuit is that it consists of only one operational transconductance amplifier (OTA) that perform all function of mixer-based beamforming (mixing, addition, and 2nd order filtering). The output function of this circuit is as follows:

$$V_{out}(s) = \frac{\frac{1}{\alpha C_1 C_c R_1^2}}{s^2 + \frac{8R_2 + R_1}{C_1 R_1 R_2} s + \frac{1}{\alpha R_1 R_2 C_c C_1}} \mathcal{L}\left(\sum_{i=1}^{8} V_{in}(t) \cdot \mathrm{sign}(I(t)[i]) \right). \quad (1)$$

Here, the transconductance of an input pair in the OTA is determined as $g_m = \frac{1}{\alpha R_1}$. We set $R_1 = R_2 = 24\mathrm{k}\Omega$, $C_1 = C_c = 33\mathrm{pF}$ to obtain quality factor $Q = 0.707$, cut-off frequency 1.25MHz, and required DR=72dB. To compensate for process variation, C_1, $C_c$consisted of capacitor banks with fourteen 3.3pF unit capacitors. Each input maximum voltage of the beamformer is limited to $100\mathrm{mV}_{pp}$ in order to reduce the requirement of the slew-rate. Fig. 3 is an illustration of the designed two-stage conventional OTA for the proposed beamformer. R_1 is set to 220 Ω to eliminate zero. The power supply voltage is 1.2V.

3. Measurement Results and Discussion

A prototype chip was fabricated on a 65-nm CMOS process. Fig. 4 present a micrograph of prototype beamformers (I and Q-Phases). The length of each side of the beamformer block is 640 μm. Resistors R_1 and R_2were arranged in the same block to reduce mismatches. Power dissipation is 0.4mW per transducer channel.

Fig.5 illustrates the measurement frequency response of the fabricated subarray beamformer. There are 9 modes caused using a capacitor bank. The result indicates that the order of the filter is 2nd from the achieved slope. Using mode 4, we can achieve the desired cut-off frequency as 1.25MHz.

Fig. 6 provides the results of addition test with 100mVpp input. This is the result of increasing the number of input signals from 1 to 8, and it can be observed that the addition is normally performed.

There are no reports as yet about the mixer-based subarray beamformer chip. Therefore, we compared our designed beamformer with the recently published time-domain beamformer [4]. The timing resolution of the chip in [4] is 25 ns. Meanwhile, it was designed that the mixer part in our system performs beamforming with a clock signal *I(t)*[*i*], which has a fine delay resolution of 5 ns. Certainly, the power consumption of the time-domain beamformer [4] is low, 0.19 mW/Ch. On the other hand, our chip has filter function and the advantages of CS can be obtained (e.g., sampling rate of an A/D converter in post-beamformer can be significantly reduced.).

4. Conclusions

A one chip 8-channel mixer-based subarray beamformer is proposed. The beamformer, which consists of mixing, addition, and filtering operations, is fabricated using a 65-nm CMOS process.

Acknowledgements

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References

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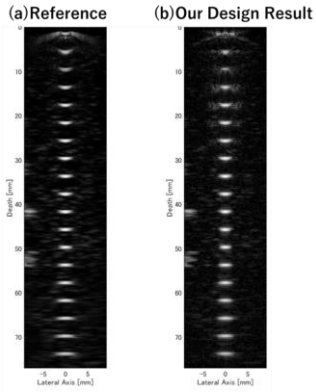


Fig.1 Ultrasound Image (Simulation).

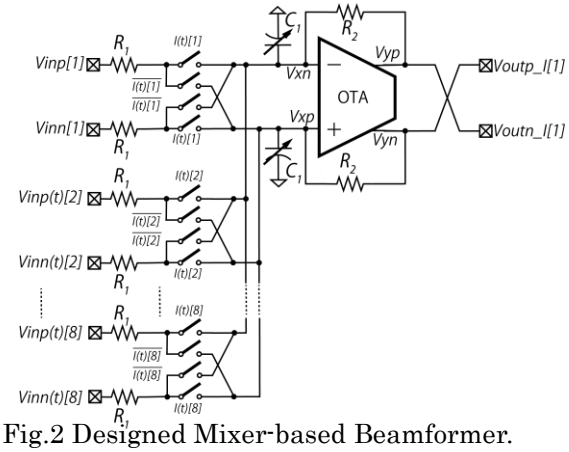


Fig.2 Designed Mixer-based Beamformer.

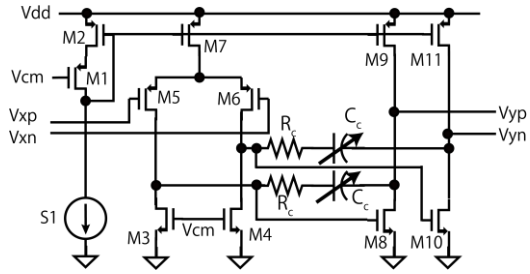


Fig. 3 Designed OTA.

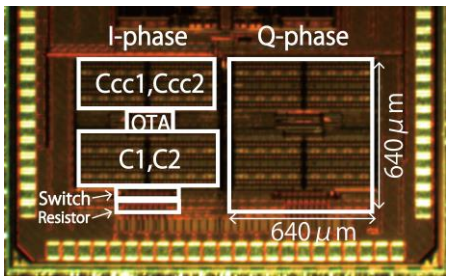
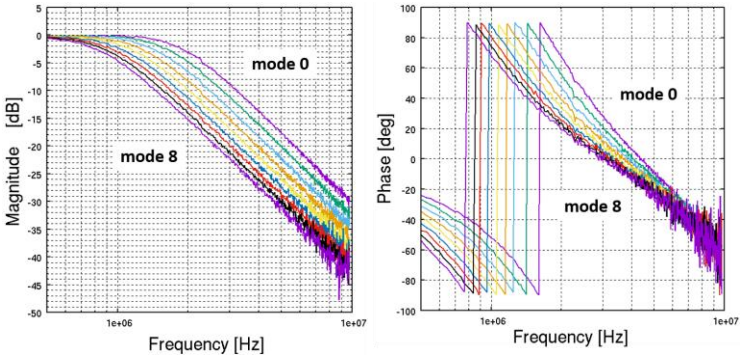


Fig. 4 Chip Die Photo.



(a) Magnitude (b) Phase

Fig. 5 Frequency response.

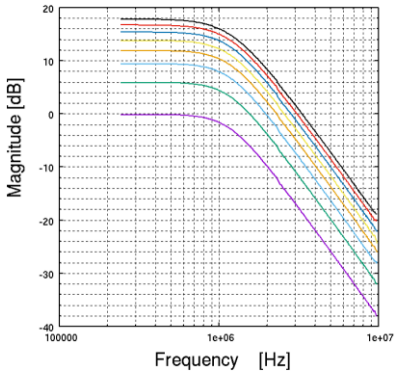


Fig. 6 Summation and Mixing results.

Table. 1 Comparison

	This work	[4]
Process (nm)	65	180
Delay Time Resolution	5ns*	25ns
Power Dissipation	0.4mW/ch.**	0.19mW/ch.***
Functions	Mixer, Adder, Filter (2nd order, BW 1.25MHz)	Analog delay Adder

*mixer timing resolution

**including I and Q both phases

*** only BDR-SCD+CDADD