Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials, VIRTUAL conference, 2020, pp3-4

A New Metric for Gauging Progress of Semiconductor Technology

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Abstract

A new metric for gauging progress of semiconductor technology is presented.

1. Introduction

Future electronic systems will continue to rely on, and increasingly benefit from, the advances in semiconductor technology as they have had for more than five decades.

Since its inception, the semiconductor industry has used a physical dimension (minimum gate length of a transistor) as a means to gauge continuous technology advancement. This metric is all but obsolete today [1]. Density (Fig. 1 – 3) is what drives the benefits of new device technologies for computation – the primary application driver for semiconductors.

2. A Density Metric for Semiconductor Technology

Going forward, we will use a three-prong metric that consists of logic density (D_L), memory bit density (D_M), and interconnect density between logic and memory (D_C) as a means to capture how advances in semiconductor device technologies enable *system level* benefits.

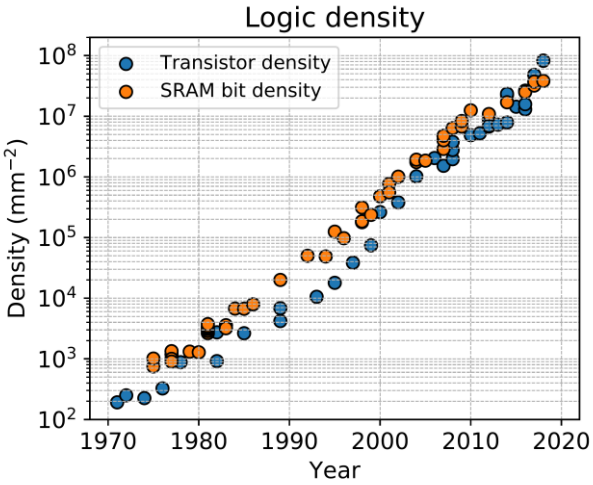

Fig. 1 Transistor density (from https://en.wikipedia.org/wiki/Transistor_count) given by the number of transistors divided by chip area and SRAM bit density (data compiled by C.-H. Fiona Wang of Stanford University [2]). After [3].

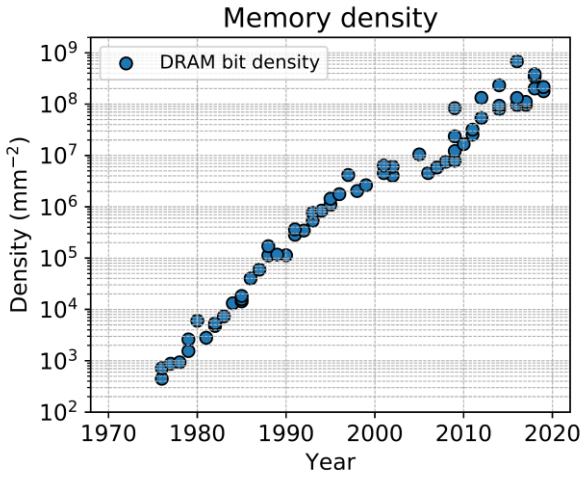

Fig. 2 DRAM bit density (data compiled by Haitong Li of Stanford University [2]). After [3].

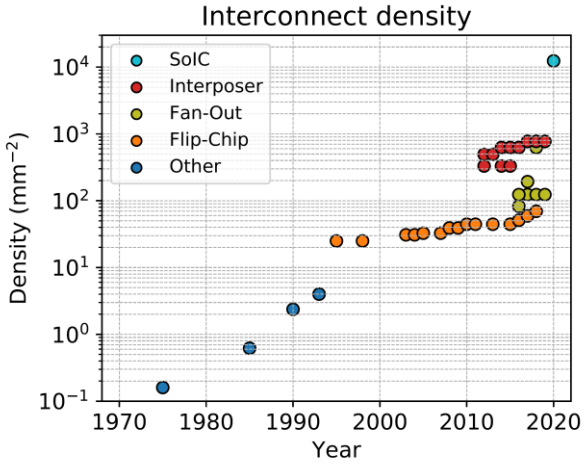

Fig. 3 Interconnect density between memory and logic (data compiled by Doug Yu of TSMC. After [3].

The proposed metric can be used to gauge advances in future generations of semiconductor technologies in a holistic

way, by accounting for the progress in logic, memory, and packaging/integration technologies simultaneously.

Acknowledgements

This work is a collaboration with researchers who are co-authors of the paper in reference [3]: Kerem Akarvardar (TSMC), Dimitri Antoniadis (MIT), Jeffrey Bokor (UC Berkeley), Tsu-Jae King-Liu (UC Berkeley), Subhasish Mitra (Stanford), James D. Plummer (Stanford), and Sayeef Salahuddin (UC Berkeley).

The author is grateful to the following colleagues and graduate students for their contributions to this article: Jin Cai (TSMC), Don C.L. Chen (TSMC), Wei-Chen (Harry) Chen (Stanford), Benson Chiang (TSMC), Haitong Li (Stanford), Shengjun (Sophia) Qin (Stanford), Mohamed M. Sabry Aly (Nanyang Technological University), Chih-Hang Tung (TSMC), Ching-Hua (Fiona) Wang (Stanford), Chuei-Tang Wang (TSMC), and Douglas Yu (TSMC). Discussions with Min Cao (TSMC), Godfrey Cheng (TSMC), Supratik Guha (U. Chicago), Thomas N. Theis (Utopus Insights), Michael Wu (TSMC), Kevin Zhang (TSMC) are gratefully acknowledged.

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